Teledyne

Junction FETs Theory and Applications

INTRODUCTION TO APPLICATION NOTES

The applications material presented on the following pages is intended for the use of the serious engineer with a basic circuit design task. It is not meant as a "hookup guide" for the casual hobbyist wishing to wire up a preamp.

Terminology used throughout these pages is consistent with that presented in the tabular data listings for various devices. Where the reader encounters a new term, he will find an explanation in the glossary elsewhere in this book.

Most of the information presented here has been developed in the application laboratories of Teledyne Semiconductor. A few sections had been published previously in technical magazines and edited or revised for this publication. Where material has been "borrowed" from outside sources, appropriate credit is appended as a note at the proper place.

Some of the most complicated design problems have the most simple solutions: if you think you know how the circuit should look, but aren't positive, you may find it expedient to obtain a sample device from a Teledyne Semiconductor sales office or representative and prepare a breadboard circuit. Strip away the symbology and you'll discover that JFETs are easy to use.

Junction FETs Theory and Applications

INTRODUCTION

The field effect transistor (FET), is a device whose operation differs radically from the NPN or PNP injection type transistor although both are called transistors. The FET is a majority carrier device while the injection type is a minority carrier device. The former is based on the properties of reverse biased pn junctions while the latter depends on a combination of reverse biased and forward biased pn junctions. Both are three terminal elements although some FET's can be made as four terminal devices without affecting the basic operation of the device.

The properties of field effect and injection transistors differs as follows:

A. Input Impedance:
   1) The FET is a high input impedance device, since the input terminal is essentially looking into a reverse biased junction.
   2) The injection type transistor is a low input impedance device because the input is basically a forward biased diode.

B. Mode of Operation:
   1) The FET is a voltage controlled device just as is a vacuum tube pentode.
   2) The injection transistor is a current controlled device.

C. Output Impedance:
   1) The FET is a high output impedance device, or current source, although different means of manufacturing may result in relatively low output impedance.
   2) The injection type transistor is also a high output impedance device, though not as "stiff" as the field effect because of the Early Effect which results in both a decreasing output impedance and a variation in gain with collector voltage.

These characteristics can be summarized in Fig. 1 which gives a comparison between typical transistors and FET's.

Fig. 1. Electrical Characteristics for (a) Injection NPN Transistor, (b) Field Effect N-Channel Transistor

MODE OF OPERATION

The three terminals of the FET are referred to as the "source," the "gate" and the "drain," corresponding to the emitter, base and collector of the transistor, respectively, or in vacuum tube terminology, to the cathode, grid and anode, respectively.

Fig. 2 shows schematically the cross section of an N-channel FET. The operation of the FET depends on the modulation of the resistance of the current path (or channel) through N type material between the source and drain contacts. This modulation is achieved by means of two P type regions (usually tied together) – the gate. When the PN junctions limiting the channel are biased in the reverse direction, the cross section of the channel is modulated by the penetration of the depletion layers of the junctions (shown by cross hatched areas in Fig. 2). Essentially no current is allowed to flow through these depletion layers except for the very small amount that constitutes the leakage of the reverse biased diodes. If the junctions are of the exponentially graded type, the penetration of the depletion layers into the channel follows a square law characteristic. When the reverse bias is so large as to cause the two depletion layers to join, the channel is said to be "pinched off," and the conductivity between source and drain drops to essentially zero.

In the normal mode of operation of the device, the source is grounded, and voltages $V_{DS}(>0)$ and $V_{GS}(<0)$ are applied to the drain and the gate, respectively. For a given combination of these voltages, the depletion layers of the PN junctions exhibit a varying width along the channel (Fig. 2b), since the back biasing voltage is essentially V_{GS} at the left hand end of the channel, and $V_{DS} + V_{GS}$ at its right hand end (neglecting voltage drops in the bulk of the source and drain regions). At sufficiently high voltages, the sum $V_{DS} + V_{GS}$ at the right hand end of the channel equals the pinch off voltage, V_P at which the channel becomes pinched off (Fig. 2c). Fig. 3 shows the drain characteristics of a typical unit, plotted for various gate voltages. The plot consists basically of two regions, the ohmic region and the pentode region. The boundary between the two regions (shown by the dotted curve) is the locus of points for which $V_{DS} + V_{GS} = V_{GS(OFF)}$. At low values of drain voltage the characteristics in the ohmic region are linear and describe the modulation of the channel conductance from its maximum

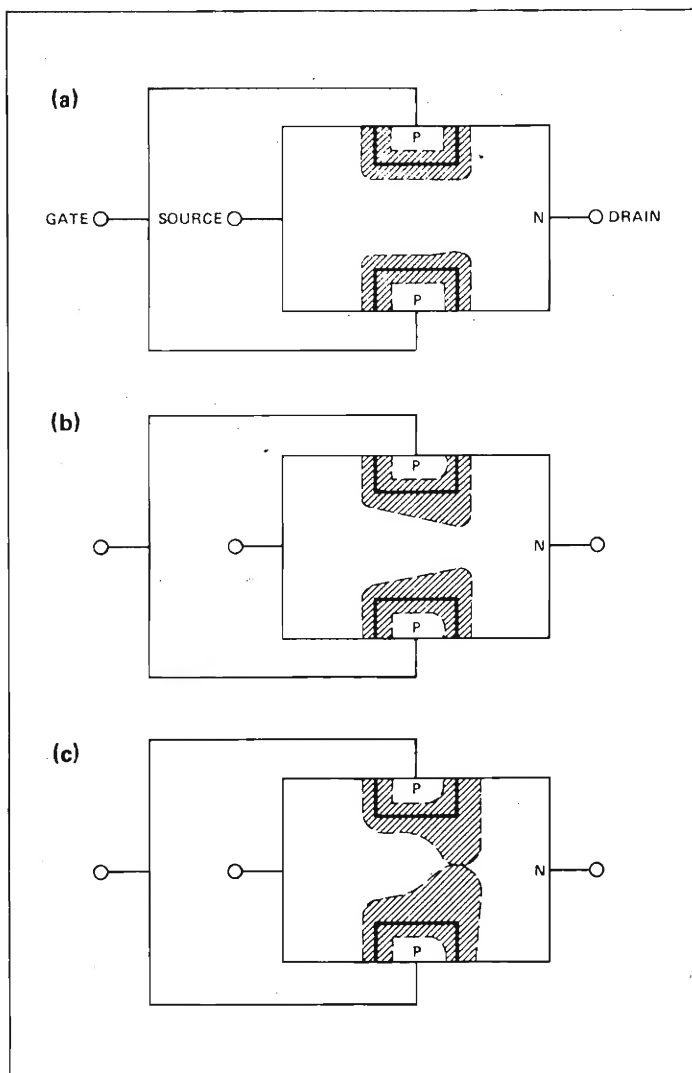



Fig. 2. Schematic Cross of Field Effect Transistor Showing Depletion Layers for
(a) $V_{DS} = 0$, $I_D = 0$;
(b) $V_{DS} + |V_{GS}| < V_P$ (Ohmic Region);
(c) $V_{DS} + |V_{GS}| > V_P$ (Pinch Off Region)

value $1/r_o$ (r_o being the channel resistance) to essentially zero when the gate voltage reaches the pinch off value, $V_{GS(OFF)}$. In the pinch off region, the channel is pinched off since $V_{DS} + V_{GS}$ exceeds $V_{GS(OFF)}$ so that further increase of current is prevented when additional drain voltage is applied. In that region, the FET can best be described as a current limiter, the amount of current being again controlled by the gate voltage.

The pinch off voltage $V_{GS(off)}$ can be deduced in two ways from the drain characteristics shown in Fig. 3, either as the voltage at which the $V_{GS} = 0$ curve saturates to a constant pinch off current I_{DSS}, or as the smallest V_{GS} value for which drain current is shut off.

The drain current at any V_{GS} can be written as:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

Another important parameter — in addition to $V_{GS(OFF)}$ and I_{DSS} — is the transadmittance Y_{fs}. It is defined in the same way as for a vacuum tube as the change of drain (plate) current with gate (grid) voltage at constant drain (plate) voltage:

$$Y_{fs} = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}} = \text{constant}$$

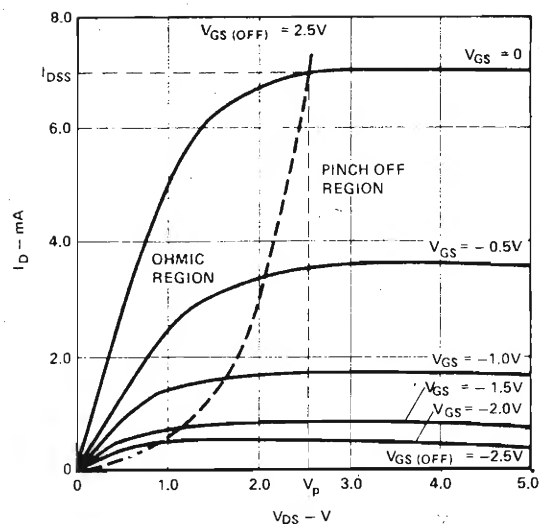



Fig. 3. Drain Characteristics of Teledyne 2N3436 Field Effect Transistor in the Low Voltage Region.

The variation of transadmittance with gate voltage is inherent to the FET and, again in the case of exponentially graded junctions, varies as

$$Y_{fs} = Y_{fso}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)$$

$$\text{where} \quad Y_{fso} = -\frac{2\, I_{DSS}}{V_{GS(OFF)}}$$

Y_{fso}, the transadmittance at $V_{GS} = 0$, is the value usually included in the specifications of the device. The approximate relation between Y_{fso} and r_{ds} is

$$Y_{fso} = 1/r_{ds}$$

The output impedance r_{ds} (similar to the plate resistance of vacuum tubes) is:

$$r_{ds} = \left.\frac{\partial V_{DS}}{\partial I_D}\right| V_{GS} = \text{constant} = \frac{1}{g_{os}}$$

Since the FET acts as current limiter in the pinch off region, r_{ds} is very high (g_{os} very low).

As is the case for transistors, the maximum reverse bias between the gate and either the source or the drain is limited by the junction breakdown voltage V_B. Breakdown characteristics have been included in the FET characteristics shown in Fig. 1, although such a range is beyond the maximum permissible voltage quoted by the manufacturer for normal operation.

Figure 4 shows a cross section similar to that of a Teledyne 2N3436 N-channel. The bottom or "back" gate is uniform, while the top or "front" gate is a series of narrow diffused strips. The isolation region surrounding the device is a deep diffusion which meets both the back and front gates and thereby electrically connects them. The device is actually made up of several channels connected in parallel by a metallization pattern over the top oxide. Each channel has its own source and drain contact; the contacts are in series (source-drain-source-drain) with a front gate separating each one. Essentially, each contact is surrounded by the front gate-isolation gate combination. The design of a channel in the bulk of the semiconductor overcomes the difficulties met in using a channel which is restricted between a gate and the surface. In the latter case, surface effects such as ionization of adsorbed impurities result in low output impedance and noisy characteristics.

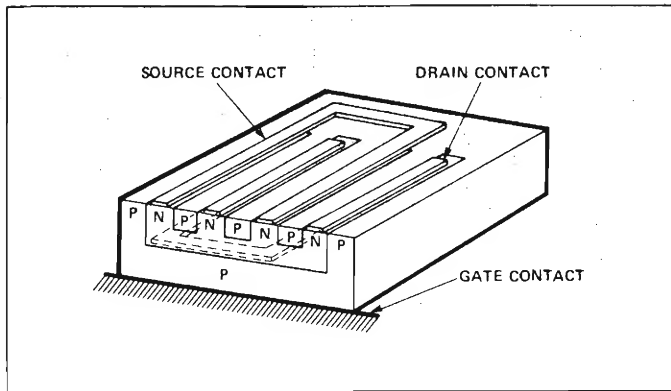



Fig.4. Simplified Cross Section of Teledyne 2N3436 Field Effect Transistor

There are two inherent properties of the FET that should be stressed here. One of the principal sources of noise in an injection transistor is the carrier recombination noise in the base. The FET is free of such noise because the current flow mechanism is determined by majority carriers (electrons in N-channels), just as in a metal conductor (typical noise figure, 1 dB). The other factor is radiation resistance. The transadmittance, g_m, of the FET, is independent of the lifetime and will therefore be relatively insensitive to radiation damage.

DESIGN PARAMETERS

The following is a summary of some of the device parameters taken on a typical Teledyne 2N3436 unit. The variation with temperature of I_{DSS}, r_o, g_{fso}, the source-to-gate leakage current I_{SGO} and the drain-to-gate leakage current I_{DGO}, are shown in Fig. 5.

The transadmittance, Y_{fs}, and saturation current, I_{DSS}, of this device have a negative temperature coefficient between 0.5 and 0.6%/°C at room temperature and vary almost linearly between −55°C and +100°C. The compensation necessary for these variations is similar to the familiar schemes used for injection transistors and will be discussed briefly later. It is interesting to note the built-in protection in the FET against thermal runaway, as an increase in temperature reduces I_{DSS} and thereby the power generated in the device.

The variation in I_{DSS} with temperature is a function of the change in material resistivity and in the change in channel thickness. The change in resistivity causes the I_{DSS} to decrease with an increase in temperature. The change in channel thickness is a result of the temperature coefficient of the depletion region and tends to open the channel up with an increase in temperature, thereby increasing I_{DSS}. The total change is written as

$$\frac{\partial I_{DSS}}{\partial T} = Y_{fso}\frac{\partial |V_{GS(OFF)}|}{\partial T} - \frac{1}{p}\frac{\partial p}{\partial T} I_{DSS}.$$

There is a point at which $\partial I_{DSS}/\partial T = 0$ given by

$$\frac{Y_{fso}}{I_{DSS}} = 3.2 \text{ volts}^{-1}$$

This can be extended to any bias point such that I_D will remain constant with temperature for a constant V_{GS} when the above condition is met.

$$I_D \simeq \frac{0.4\, I_{DSS}}{V_{GS(OFF)2}} \text{ or } V_{GS\,z} \simeq (V_{GS(OFF)})\ 0.64 \text{ V}$$

Both leakage currents I_{SGO} and I_{DGO} follow the theoretical dependence on temperature of diffused PN junctions in silicon, the small difference in leakage currents at the same

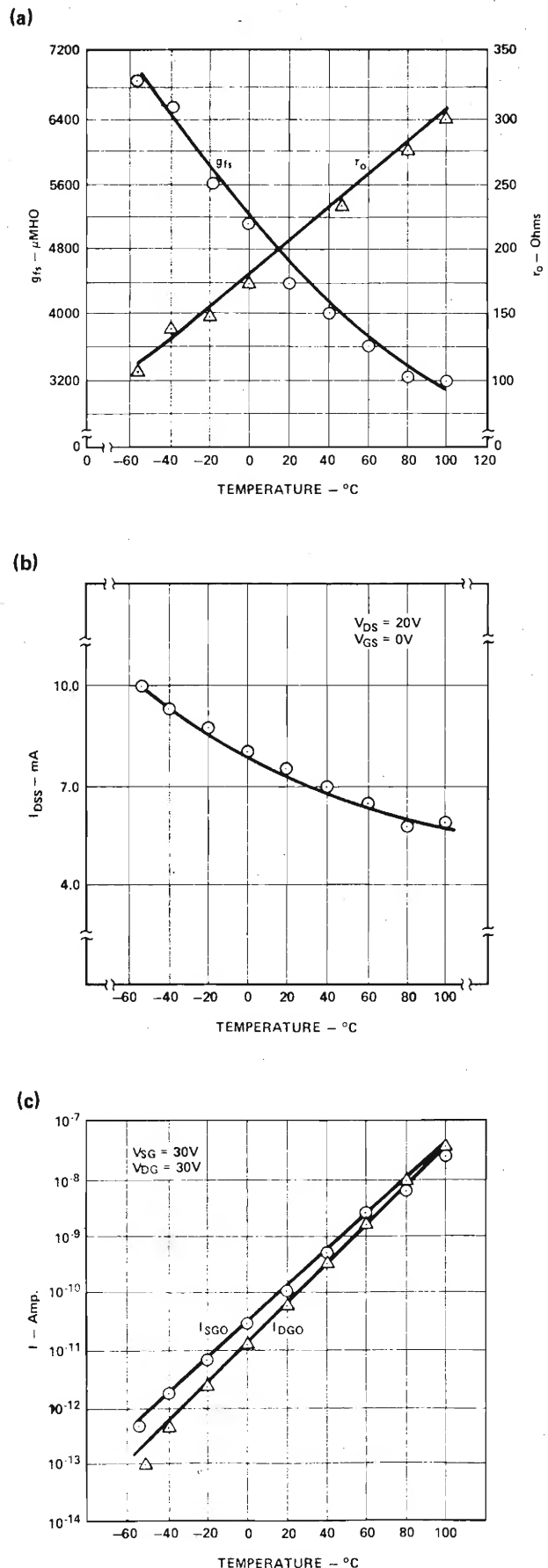



Fig. 5. Temperature Dependence of
(a) Transconductance, Y_{fs} and "on" Resistance, r_o;
(b) Pinch Off Current, I_{DSS}
(c) Source and Drain Leakage Currents, I_{SGO} and I_{DGO}

temperature being due to the geometry of the junctions. Another parameter which is of interest is the variation of gate to drain and gate to source capacitance as shown in Fig. 6.

In addition to a $V^{-1/3}$ variation in capacitance above and below pinch off, we observe a rapid variation of capacitance with voltage at the pinch-off voltage. This is due to the fact that below pinch-off, the capacitance is that of the entire gate junction, whereas above pinch-off it is only the capacitance of the drain or the source isolated from each other.

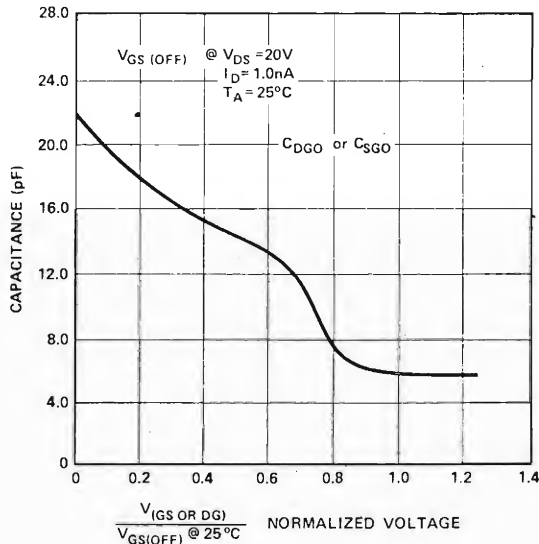



Fig. 6. Variation of Source to Gate and Drain to Gate Capacitance with Normalized Bias

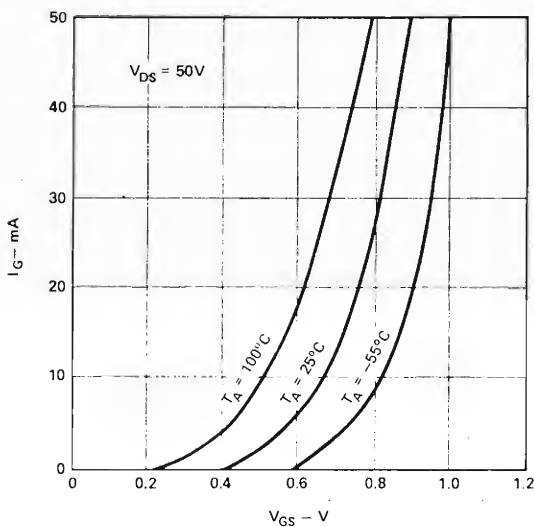



Fig. 7. Temperature Dependence of Forward Biased Gate Characteristics

In view of the possibility of allowing the gate to be positively biased with respect to the source, the plot of gate current vs. gate-to-source voltage is given in Fig. 7 for various temperatures. Except for gate current as shown, the device will operate in the normal way (i.e., no flow of current from drain to gate except for leakage current) so long as the drain voltage is not allowed to become more negative than the gate. This, of course, is a relatively simple matter since the gate voltage cannot exceed that of a typical forward biased diode whereas the useful range of the device is at much higher drain voltages.

APPLICATIONS OF FIELD EFFECT TRANSISTORS TO AMPLIFIERS

Figure 8 shows the biasing of a field effect transistor as well as of a vacuum tube pentode to illustrate the analogy. The biasing may vary widely with the application, the most common being the grounded source configuration as shown.

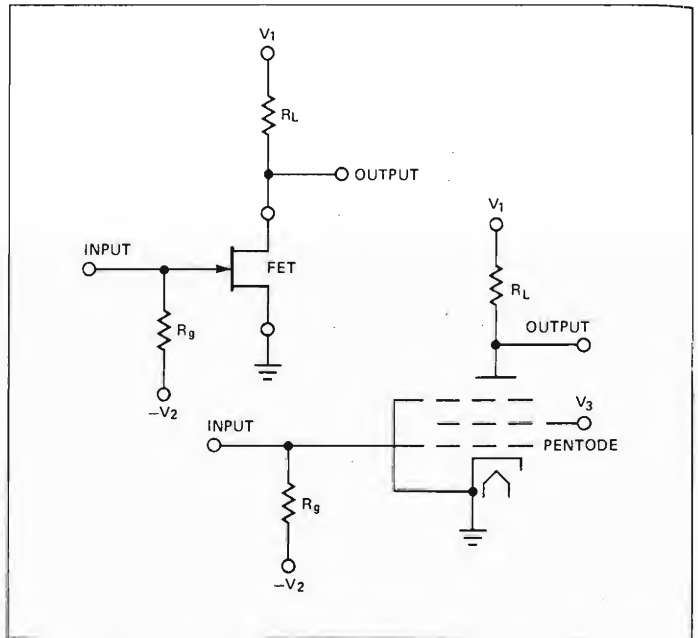



Fig. 8. Analogy Between an FET and a Pentode Circuit

The expression for the gain of such an amplifier is

$$A_V = \frac{\mu R_L}{r_{ds} + R_L} = \frac{Y_{fs} r_{ds} R_L}{r_{ds} + R_L} = \frac{Y_{fs} R_L}{1 + R_L g_{os}}$$

where

$\mu = Y_{fs} r_{ds}$.

If $r_{ds} >> R_L$ the expression for voltage gain reduces to:

$A_V = Y_{fs} R_L$ at low frequencies.

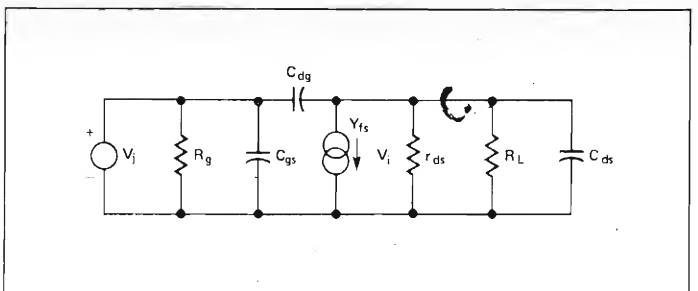



Fig. 9. Small Signal Equivalent Circuit of an FET

The small signal equivalent circuit is shown in Fig. 9. Because of the variation of Y_{fs} with V_{GS}, the requirement for maximum gain indicates the desirability to operate close to $V_{GS} = 0$. This brings up the question of the possibility of biasing the gate in such a way that the latter is at ground potential in the quiescent state. Such an operation is possible since a forward biased gate junction does not conduct appreciable current (thereby reducing the input impedance

drastically) until a positive voltage of about 0.3 volts is reached. Depending on the amplification and signal levels at any given gate input, the DC bias may be picked slightly negative with respect to the source.

Figure 10 shows a simple circuit for an AC amplifier designed for a gain of 2×10^3.

We will assume that FET_1 and FET_2 are identical with $V_{GS(OFF)} = -2.0$ volts, $I_{DSS} = 3$ mA, $Y_{fso} = 4000$ μmhos and $g_{os} = 10$ μmhos. This circuit will be designed so that the gate of FET_1 is at ground ($V_{GS1} = 0$) and the gate of FET_2 is at −1 volt ($V_{GS2} = -1$ V). For a gain of 40 for the first stage, the load at the drain must be 11.1 k and this can be calculated as

$$R_L = \frac{A_V}{Y_{fs} - A_V g_{os}} = \frac{40}{(4000\text{-}400)\ 10^{-6}}$$

$$= \frac{R_1 \times R_2}{R_1 + R_2}$$

$$= 11.1\ \text{k (assuming } X_{C1} << R_1 + R_2\text{)}.$$

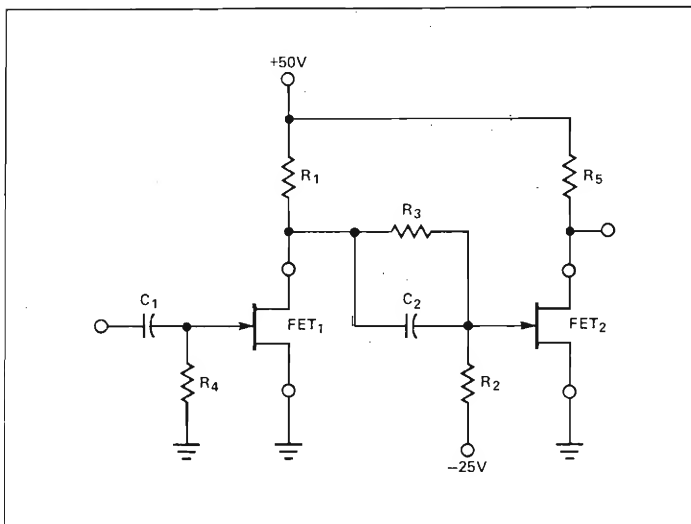



Fig. 10. FET Amplifier Circuit

At steady-state, $I_{D1} = 3$ mA, and $V_{GS2} = -1$ V. Therefore, if R_2 and R_3 are much greater than R_1, then $R_1 = 11{,}000$ ohms. Furthermore, since the DC loading of R_2 and R_3 can then be neglected, $V_{DS1} = 17$ volts and

$$\frac{R_2 \times 42}{R_2 + R_3} = 18.$$

Letting R_2 be 1 Meg gives a value for R_3 of approximately 0.75 Meg. The value of R_5 can now be determined from the overall gain of 2×10^3. Therefore, $Y_{fs2}R_5$ must equal 2×10^3/40 or 50. But Y_{fs2} is

$$Y_{fs2} = Y_{fso}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right) = 4000\ (1 - 0.5)$$

$$= 2000\ \mu\text{mhos}$$

giving a minimum value for R_5 of 33,000 ohms. It will be noted that R_5 can be made larger to obtain still higher gain, the choice being determined by the maximum voltage swing desired at the output and the harmonic distortion that can be tolerated. However, the advantages of using a high voltage device to achieve higher gains are readily apparent.

For maximum voltage gain at the same power level, the usable voltage gain is that region of the device between the gate cutoff voltage $V_{GS(OFF)}$ and the maximum supply voltage. V_I. This indicates a figure of merit $(g\,V_A)/I$, where V_A is the available voltage swing or $V - V_{GS(OFF)}$. Since the maximum load resistance that can be used is V_A/I_{DSS}, the maximum gain available is

$$\frac{Y_{fs}}{g_{os} + \frac{I_{DSS}}{V_A}}$$

(This number might be typically 100). This figure of merit is especially interesting from two points of view: 1) A unit having a large Y_{fs} and V_A, as shown in this example, and a low I_{DSS} and g_{os}, can be used in almost any present day electronic application where voltage gain and power gain are a prerequisite, so that the larger this number is, the greater the advantages and flexibility. 2) Even though FET units have been made in the past with rather large transadmittance (50 to 100 mmhos) their scope in practical circuits has been limited because of either a small V_A or large I_{DSS} or both. Such units have been limited to applications that can tolerate a voltage gain less than unity.

In small signal applications, the frequency limitation of this device is determined by the Miller capacitance as shown in the equivalent circuit given in Fig. 9. There is no other practical frequency limitation because the field effect is a majority carrier device in contrast with the injection transistor which is a minority carrier device.

Referring to Fig. 9, we see that the input impedance will decrease with increasing frequencies at which the quantity $1/2\pi C_{is}$ becomes comparable to the input resistance. Furthermore, the gain bandwidth product will be approximately:

$$\text{Gain bandwidth} = \frac{Y_{fs}}{2\pi C_{is}}$$

This dictates a direct compromise between circuit gain and bandwidth as is well known in network theory. Since Y_{fs} and C_{is} both decrease with increasing bias voltage, V_{GS}, it is interesting to investigate the effect on gain-bandwidth figure of merit. As V_{GS} is increased (more negative for N channel), the gain-bandwidth product has a slight peak at about 15% of gate cutoff voltage, $V_{GS(OFF)}$. However, the product is essentially constant for values of V_{GS} less than about 30% of $V_{GS(OFF)}$.

SWITCHING APPLICATIONS

These applications refer to the case where, in analogy to the injection type transistor, the device is either "on" or "off." The parameters of interest here are the transadmittance, the "off" current and the "on" impedance, r_{ds}. The "off" current is the drain current when the unit is biased beyond pinch-off and is of the order of the leakage currents. The "on" impedance, r_{ds}, is the slope of the curves in Fig. 3 in the region between $V_D = 0$ and $V_D = V_{GS(OFF)}$

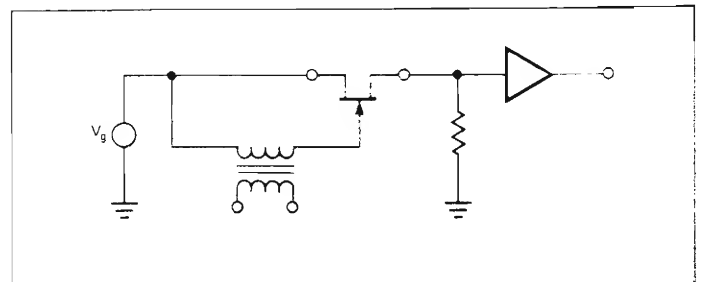



Fig. 11. FET Chopper Circuit

There are switching applications such as in choppers where the field effect transistor is very much superior to the conventional transistor. When used in an unbalanced

configuration as in Fig. 11, the offset voltage when the unit is turned off would be of the order of 200 microvolts or at least one hundredth of the offset voltage that would result if an injection type transistor were used.

In the latter case, the offset voltage is primarily a function of the transport factor of the transistor and is therefore fairly high. It might be of the order of 50 mV in the normal and 5 mV in the inverse configuration at zero load current, whereas this voltage is zero in the FET because the drain to source characteristics start right at the origin. The offset voltage at zero load current would therefore be zero. The offset voltage when the unit is shut off is determined (as quoted) by the leakage current and the load impedance as in conventional injection type transistors. If one were to use matched pairs to cancel the offset due to the leakage currents, this improvement in addition to the true zero offset in the "on" condition makes the FET chopper applicable in low level circuits where mechanical relays have had to be used in the past. Junction capacitance is important in switching circuits since it limits the turn-on and turn-off times when switching into a given load resistance, R_L. The "on" resistance of the FET is also important in switching circuits since it determines the size of the load resistance and therefore the switching time.

GENERAL CHARACTERISTICS

Shown in Fig. 12 are the specifications for the Teledyne 2N3436 and 2N3967 field effect transistors. These specifications may be referred to when studying the curves that follow to get an indication of the actual range of the parameters.

Typical drain current families are shown in Figs. 13a and 13b. These curves are of limited use in circuit design (as are the grounded emitter collector current families for injection transistors), but are included to show their similarity to vacuum pentode characteristics.

Figures 14a, 14b, 15a and 15b show the temperature dependence of drain current, I_D and transadmittance, Y_{fs}, as a function of gate to source voltage, V_{GS}. These characteristics are normalized and their usefulness in circuit design will be shown in examples given in a later section.

DC BIAS CONSIDERATIONS

In this section we consider the problem of biasing a grounded source amplifier stage at a particular operating point and maintaining the operating point within specified limits as the temperature varies or as different devices are placed in the circuit. Three circuits will be considered: 1) A grounded source amplifier without feedback, 2) an amplifier with source degeneration, and 3) an amplifier with drain to gate feedback.

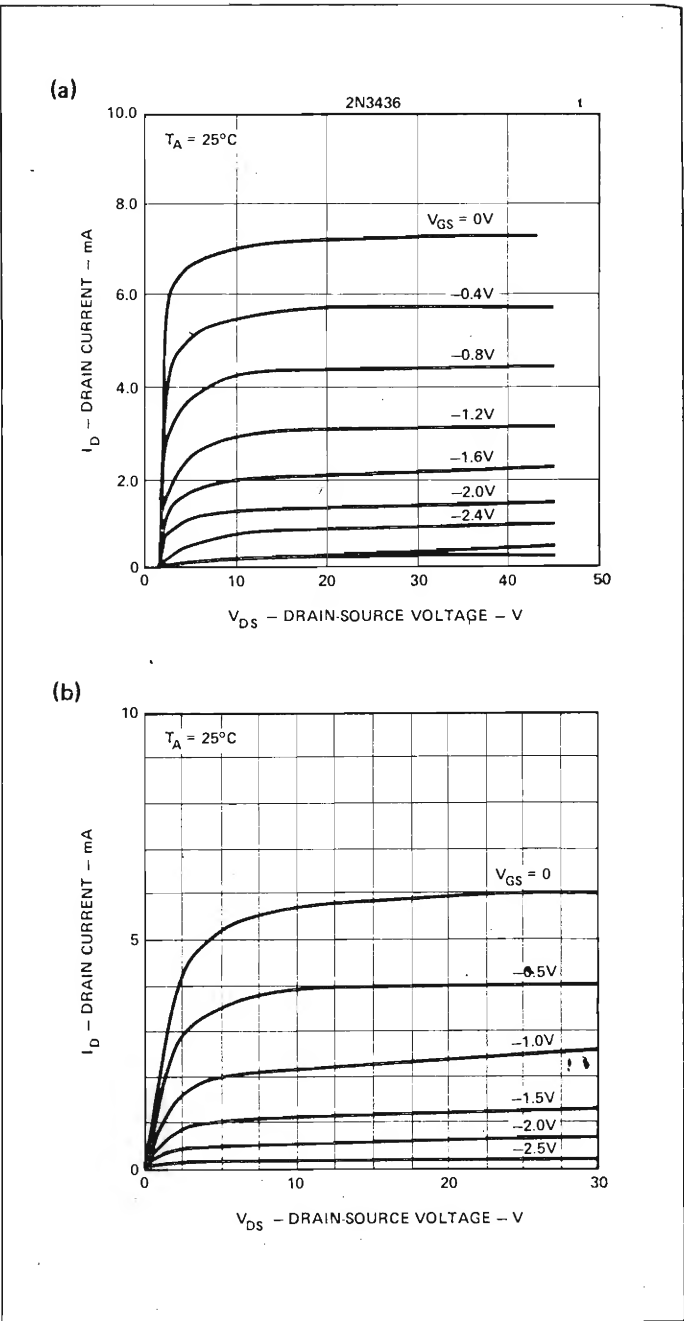



Fig. 13. Typical Field Effect Drain Current Families

		2N3436				2N3967			
Symbol	Characteristic	Min.	Max.	Units	Test Conditions	Min.	Max.	Units	Test Conditions
BV_{DGO}	Drain to gate breakdown Voltage	50		Volts	$I_D = 1.0\ \mu A$, $I_S = 0$	30		Volts	$I_D = 1.0\ \mu A$, $I_S = 0$
I_{GSS}	Total gate leakage current		0.5	nA	$V_{DG} = 30$ V, $V_{DS} = 0$		0.1	nA	$V_{DG} = 20$ V, $V_{DS} = 0$
$I_{GSS}(150°C)$	Total gate leakage current		1.0	μA	$V_{DG} = 30$ V, $V_{DS} = 0$		0.2	μA	$V_{DG} = 20$ V, $V_{DS} = 0$
I_{DSS}	Saturation current	3.0	15	mA	$V_{DS} = 30$ V, $V_{GS} = 0$	2.5	10	mA	$V_{DS} = 20$ V, $V_{GS} = 0$
Y_{fs}	Transadmittance	2500	10,000	μmhos	$V_{DS} = 30$ V, $V_{GS} = 0$	1600	2400	μmhos	$V_{DS} = 20$ V, $I_D =$ [illegible]
$V_{GS(OFF)}$	Gate cutoff voltage		10.0	Volts	$V_{DS} = 20$ V, $I_D = 1.0$ nA		5.0	Volts	$V_{DS} = 20$ V, $I_D = 1.0$ nA
C_{dg}	Drain to gate capacitance		5.0	pF	$V_{DG} = 10$ V, $I_S = 0$		1.3	pF	$V_{DG} = 10$ V, $I_S = 0$
C_{sg}	Source to gate capacitance		5.0	pF	$V_{SG} = 10$ V, $I_D = 0$		1.5	pF	$V_{SG} = 10$ V, $I_D = 0$

Fig. 12.

(a) 2N3436 V_{DS} = 30V

I_D/I_{DSS} (25°C) vs. $\left|\frac{V_{GS}}{V_{GS(OFF)} @ 25°C}\right|$ — curves: −55°C, 25°C, 125°C

(b) 2N3967 V_{DS} = 30V

I_D/I_{DSS} (25°C) vs. $\left|\frac{V_{GS}}{V_{GS(OFF)} @ 25°C}\right|$ — curves: −55°C, 25°C, 125°C

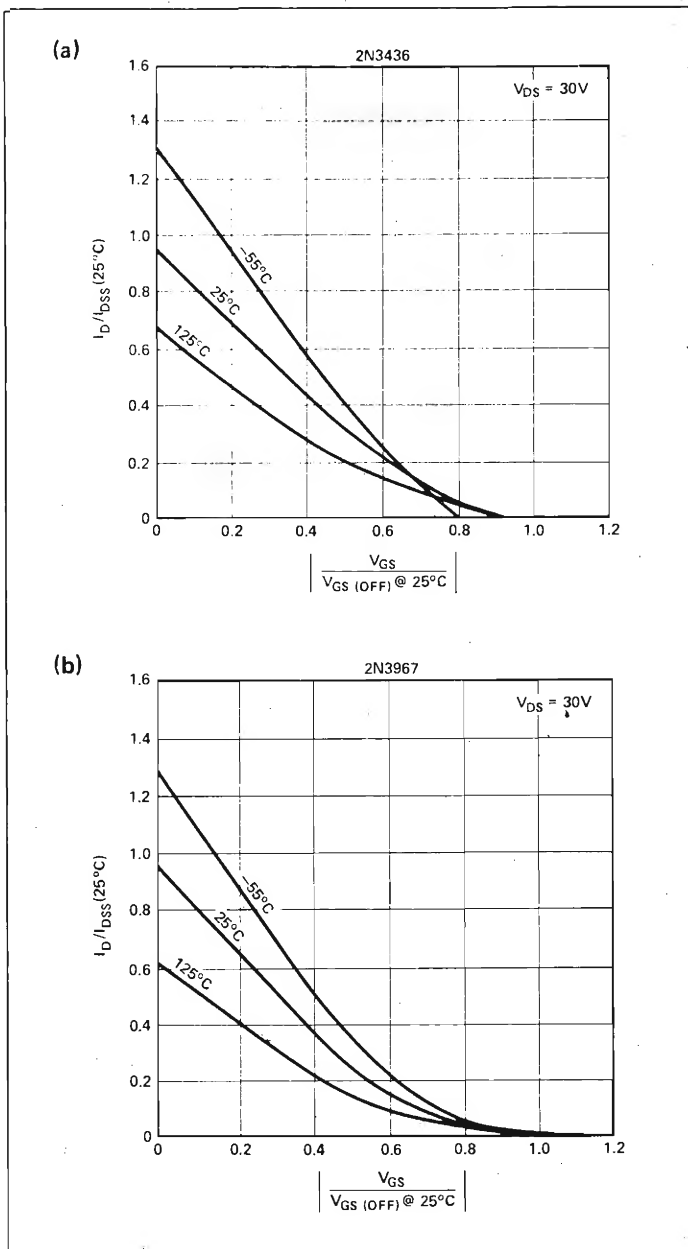



Fig. 14. Normalized Transfer Characteristics

(a) 2N3436 V_{DS} = 30V

Y_{fs}/Y_{fso} (25°C) vs. $\left|\frac{V_{GS}}{V_{GS(OFF)} @ 25°C}\right|$ — curves: −55°C, 25°C, 125°C

(b) 2N3967 V_{DS} = 30V

Y_{fs}/Y_{fso} (25°C) vs. $\left|\frac{V_{GS}}{V_{GS(OFF)} @ 25°C}\right|$ — curves: −55°C, 25°C, 125°C

Fig. 15. Normalized Transconductance vs. Gate to Source Voltage

Shown in Fig. 16 is a grounded source amplifier. The FET transfer characteristics representing extremes with respect to temperature and devices are shown in Fig. 17 by the curves C_1 and C_2. Consider first the case with $R_S = 0$ (no degeneration) and a bias voltage V_{GG}. The change in drain current ΔI_D will take place along the $R_S = 0$ load line as indicated in the figure. It can be seen that the amount of this change can be quite severe in many applications.

V_{DD}, R_L, R_G, R_S, V_{GG}

Fig. 16. Grounded Source FET Amplifier

I_D, ΔI_D, $-I_D$, $R_S > 0$, $R_S = 0$, C_2, C_1, 0, V_{GS}, V_{GG}, V_{GG1}

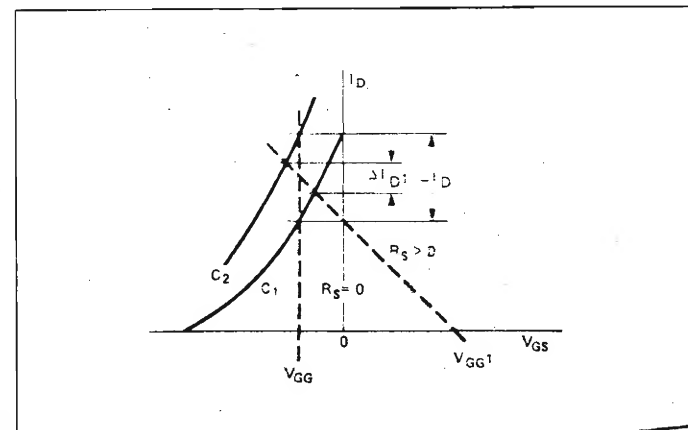



Fig. 17. Transfer Characteristics

For the case of $R_S > 0$ (source degeneration) with the same initial operating point, the R_S load line will be as shown in Fig. 16. The bias voltage for this condition is now V_{GG}'. The change in drain current $\Delta I'_D$ occurs along the $R_S > 0$ load line and is reduced over the $R_S = 0$ case by the amount indicated. Theoretically, we can make R_S as large as we please to minimize the shift in the operating point with temperature and with different devices in the circuit. The practical limit on the size of the R_S is determined by the bias voltage available and by the required low frequency gain. The low frequency voltage gain with source degeneration is

$$A_V = \left[\frac{Y_{fs}R_L}{1 + Y_{fs}R_S + g_{os}(R_L + R_S)}\right]$$

where

Y_{fs} is the transadmittance at the operating point

g_{os} is the output conductance at the operating point

$$A_V \approx \frac{Y_{fs}R_L}{1 + Y_{fs}R_S} \approx \frac{R_L}{R_S} \text{ for } Y_{fs}R_S >> 1$$

An amplifier with drain to gate feedback is shown in Fig. 18. Assume that the direct current flowing through R_1, R_2 and R_3 is much smaller than the current I_L flowing through R_L. Also, we will neglect the junction leakage currents. Then

$$I_D \simeq I_L$$

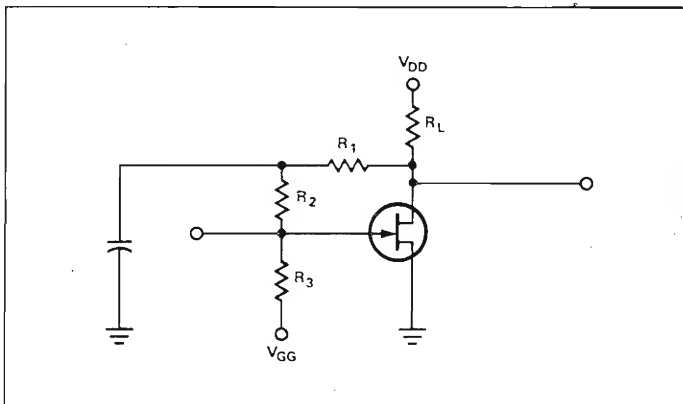



Fig. 18. Grounded Source Amplifier with Drain to Gate Feedback

Now consider a small change in the drain current. Then

$$\Delta V_{GS} \simeq \frac{R_3R_L}{R_1 + R_2 + R_3}\Delta I_D.$$

Let

$$R_T = \frac{R_3R_L}{R_1 + R_2 + R_3}$$

Then

$$\frac{\Delta I_D}{\Delta V_{GS}} \simeq \frac{1}{R_T}$$

The transfer characteristics' extremes shown previously are again shown in Fig. 19. As an example, let us assume that the maximum allowable shift in drain current is as shown in the figure. The R_T must be equal to or greater than the reciprocal of the slope of the line connecting the two points of intersection of the maximum and minimum drain currents and the transfer characteristics.

In the preceding discussion on biasing considerations we have used the regular characteristics rather than the normalized characteristics for the sake of clarity. The normalized characteristics can, of course, be used if the load lines are properly normalized to

$$\frac{V_{GS(OFF)}(25°C)}{I_{DSS}(25°C)}$$

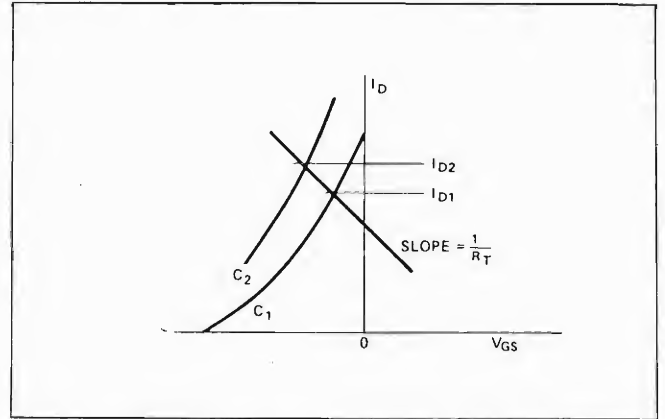



Fig. 19. Transfer Characteristics

for the particular devices used. We have also neglected the change in drain current with the change in drain to source voltage. This change, however, is small compared to the change due to temperature and the normal variation in drain current characteristics from one device to another

The three biasing methods shown are the basic methods used in vacuum tube and transistor circuit design. Where greater operating point stability is required, more elaborate forms of biasing and compensating will have to be employed.

APPLICATION OF PAIRS

In this section, two examples of FET amplifier circuits are given to show how FET pairs can be used to some advantage. The examples given are in simple form, but can be extended and applied in more complex configurations as specified applications are considered.

The voltage gain of the circuit shown in Fig. 16 was given as

$$A_V = \left[\frac{Y_{fs}R_L}{1 + Y_{fs}R_S + g_{os}(R_S + R_L)}\right]$$

The gain for a given FET amplifier is limited by the size of R_L. However, to insure operation in the pinch-off region where the gain is a maximum,

$$R_L < \frac{V_{DD} - |V_{GS(OFF)}|}{I_D}$$

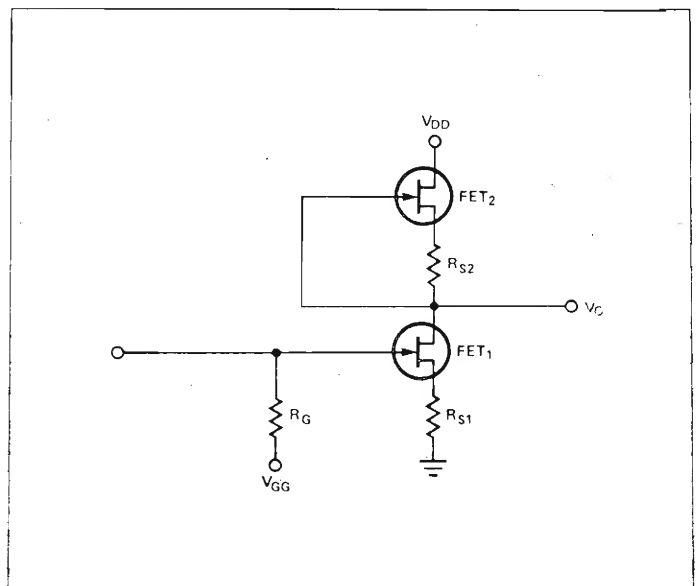
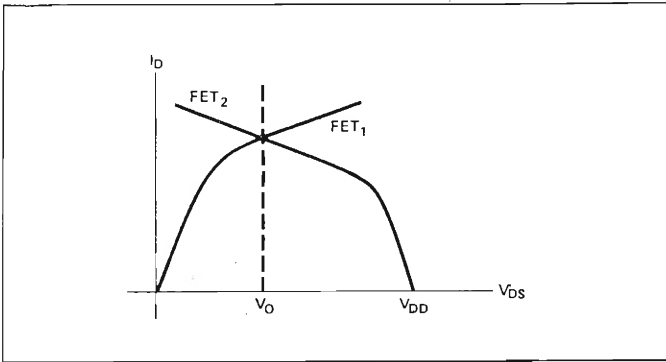



Fig. 20. A Two FET Amplifier

Figure 20 shows a two FET amplifier designed to give maximum voltage gain with a limited supply voltage V_{DD}, and some temperature stability. Here the load resistance has been replaced by another FET. The operation of this circuit is best shown by the grounded source characteristics in Fig. 21. The load is now effectively the drain resistance of the upper FET, $1/g_{os2}$. The gain for this configuration is

$$A_V = \frac{Y_{fs1}}{g_{os1} + g_{os2} + R_{S1}(Y_{fs1}g_{os2} + g_{os1}g_{os2})}$$
$$\approx \frac{1}{R_{S1}g_{os2}}$$

21. Two FET Amplifier Characteristics

This circuit has the advantage of improved operating point stability if the drain currents of both FET's have approximately equal temperature co-efficients. For best operation, the characteristics of the two devices (in particular, I_{DSS} and V_P) should be closely matched.

Field effect source followers can be used in the same manner as vacuum tube cathode followers and transistor emitter followers. A typical source follower circuit is shown in Fig. 22. Shown in Fig. 23 is the transfer characteristics for the FET. Consider the case of $V_{SS} = 0$. The voltage gain of the source follower is

$$A_V = \frac{Y_{fs}R_S}{1 + R_S(Y_{fs} + g_{os})} \approx \frac{Y_{fs}R_S}{1 + Y_{fs}R_S}$$

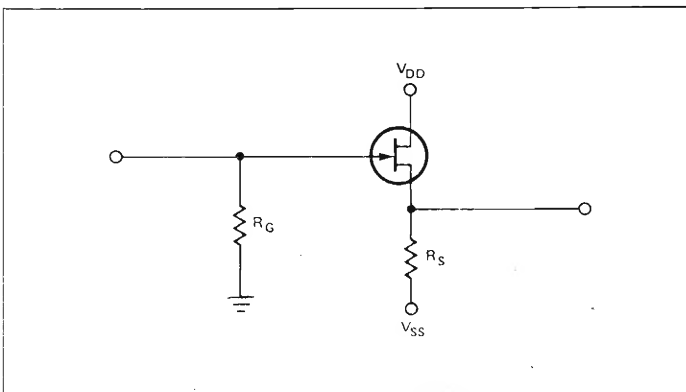



Fig. 22. FET Source Follower

To approach unity gain, $Y_{fs}R_S$ must be much greater than one. We can make R_S large, but as we increase R_S, the operating point moves down the transfer characteristics to the region where Y_{fs} is low (refer to Figs. 15a and 15b, Y_{fs} vs. V_{GS}). Therefore, for $V_{SS} = 0$ the voltage gain is much less than unity. By making V_{SS} negative, the R_S load line is

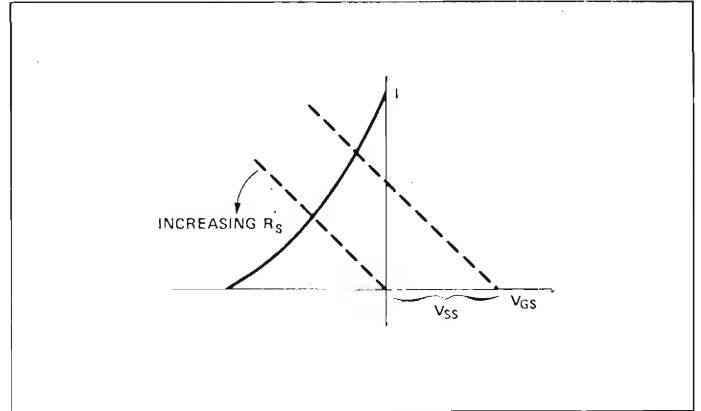



Fig. 23. Transfer Characteristics

translated to the right as indicated in Fig. 23. The voltage gain is increased since the operating point is moved up the transfer characteristics where the Y_{fs} is higher, thus increasing $Y_{fs}R_S$.

Shown in Fig. 24 is a two FET source follower. Here we have replaced the load resistor with a field effect constant current load. The operating point of the upper FET is determined by the drain current of the lower FET. This configuration requires that the I_{DSS} of the upper FET must be less than that of the lower. The output impedance of this circuit is approximately $1/Y_{fs2}$. This circuit also has the advantage of improved operating point stability since the drain currents of both FET's vary with temperature in a similar manner.

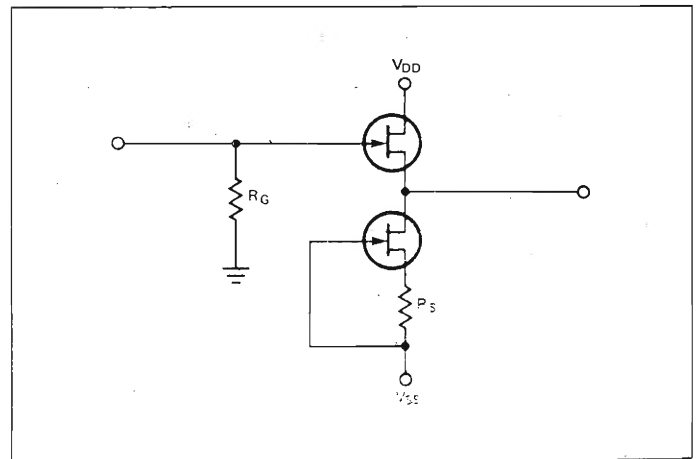



Fig. 24. Two FET Source Follower

NOISE CHARACTERISTICS OF FIELD EFFECT TRANSISTORS

The fundamental limitation of the sensitivity of any network is set by the amount of noise generated by that network. Noise, irrespective of the source or mechanism of its generation, has the dimensions of power (i.e., $P_n = KTB$) and is characterized by its random or uncorrelated behavior with time. When the signal power fed into the input of an active network is decreased beyond a certain level, the signal at the output of the network is no longer recognizable in the noise generated within the network.

The generation of noise is associated with all physical devices whether active or passive. Field effect transistors (FET) like all devices are subject to a physical environment and exhibit several types of noise. The difference is that,

under some operating conditions, FET's exhibit noise behavior superior to transistors and vacuum tubes.

In applications requiring low noise amplification below 500 Hz, the low noise characteristics of the Teledyne FET are particularly suitable because of its low l/f noise. The FET has many of the better features of the vacuum tube such as high input impedance and transadmittance without the higher l/f noise, does not require a high plate voltage or a filament supply, and the FET is not microphonic.

Popular junction FET's for varying application — N-channel unless otherwise noted.

1. High Voltage (guaranteed BV_{DGO} greater than 150 to 300 V) 2N4881-6; AN5277-8.
2. Low Noise (low e_n guaranteed) 2N5391-6.
3. Switching (guaranteed r_{ds} less than 5-100 ohms) 2N3970-72; 2N4091-3; 2N4391-3; 2N5432-4; 2N4856-6 2N4977-9; 2N5018-9 (P-channel); P1086-7E (P-channel U1897-9E (N-channel).
4. High Frequency Amplifier and Mixers (200-500 MHz operation) 2N4416; 2N3823; 2N4223; 2N5078; U1994 U2047E, U1837E.
5. Low Leakage Amplifiers (less than 1-5 pA input current) 2N5647-9; U1714.
6. General Purpose N-Channel Amplifiers, 2N3436-2N3821-3; 2N3966-9; 2N4220-4; 2N4302-4 (Epoxy).
7. General Purpose P-Channel Amplifiers 2N2606-9.
8. Dual Matched FET's 2N5045-7; SU2365-9. A 2N5196-2N3954-6; 2N3921-2; 2N4084-5; 2N3934-5; 2N4082-TD5902-9.

Junction FET Analogies and Parameter Tradeoffs

Quite frequently, a specification will be written combining the best of several different devices into one that, with present technology, is impossible to manufacture. All that is usually lost here is valuable time and a lot of wasted effort. Other times, a specification reflects a 2-3% yield item which was not the intent in the first place. This misunderstanding becomes costly via the "Cadillac" price on a required "Volkswagen" item.

It is not necessary to know every little theoretical detail of the device physics and design equations involved in JFETs, but a logical concept of parameter interactions and tradeoffs will help in making parameter selections and combining device specs.

JFET Analogies

For those not familiar with FET analogies and tradeoffs, the following discussion gives the beginner a working knowledge based on logic for FET characteristics.

For a working model, let's consider a common garden hose, its characteristics, interactions, and tradeoffs. Essentially the same problems arise in designing and selecting FETs.

1. **I_{DSS}** (Drain Saturation Current) — All JFETs are depletion mode type — normally "on" when no bias is applied. I_{DSS} is similar to the measurement of gallons/hr. flow through the hose. Up to a point, I_{DSS} increases with increasing voltage, just as water flow increases with line pressure, then the flow limits.

2. **$V_{GS(OFF)}$** (Gate-Source Cutoff Voltage) — the required bias voltage to shut off the FET is like measuring how far the faucet valve needs to be shut, to stop the flow. Interestingly it is essentially independent of applied pressure (voltage).

3. **Y_{FS}** (Forward transadmittance) — By definition, it is the quantity change in drain current for the quantity change in gate-source voltage, $Y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS} = K}$, or a ratio of change of water flow in relation to a defined change in faucet opening.

4. **I_{DSS}, $V_{GS(off)}$, Y_{FS} Interactions**
For a JFET, an interaction exists between the three key parameters, namely $Y_{FS} \doteq \frac{2I_{DSS}}{V_{GS(off)}}$. As the garden hose inside diameter increases, more water can flow per hour (I_{DSS}), but also the greater distance the full size non restricting hose faucet would have to be shut off $V_{GS(off)}$ Similarly, the greater change in water flow for a given faucet adjustment (Y_{FS}). i.e. Fire hydrant and hose versus ¾" faucet and hose.

5. **$V_{(BR)GSS}$** — Gate-Source Breakdown Voltage
This is the maximum source &/or drain junction operating voltage. How many PSI the hose will handle before it breaks.

6. **I_G, I_{GSS}** — Gate Leakage Current
A measure of how perfect the junction is. The amount of water leakage at the valve connection or pin holes along the hose.

7. **Y_{OS}** — Output Admittance
A measure of the inverse of the slope of the drain current as the Drain-Gate voltage is increased. Small because, like the hose, beyond a certain line pressure little extra water flows for a further increase in pressure.

8. **r_{DS}** — Drain "ON" resistance
A measure of the non-biased channel "ON" resistance. Simply is the familiar $r_{DS} = \frac{pL}{A} = \frac{pL}{2aZ}$ (Fig. 1). The higher the device $V_{GS(off)}$, for a given family, the lower the r_{DS}. The larger the inside diameter of a hose, the lower the resistance to the water flow.

9. **C_{iss}, C_{rss}** — Input Capacitance, Reverse Transfer Capacitance
A measure of the active area of the FET. Simply a reading of $C \doteq \varepsilon \frac{A}{D}$. Devices with higher I_{DSS}, lower r_{DS} for a $V_{GS(off)}$ generally have higher capacitance. Similarly the hose that handles more water/hr. will have a larger outside diameter.

10. **I_{DSS}, r_{DS}, Y_{fs}, $V_{(BR)GSS}$ Interaction**
By keeping the same size device (C_{iss}, C_{rss} = Constant), by narrowing the drain to gate spacing, we lower the breakdown and increase the current capacity. A two inch O.D. hose may have 1/16" thick walls or even 1/4" thick walls, greatly varying the water flow rate.

Parameter Tradeoffs

Just as we can design hoses in various ways; greater outside diameter, thinner walls, stronger material, oval rather than round, several circular hoses connected in parallel, less leaky connectors, FET Design is a compromise to optimize those parameters that are critical at the expense of others.

Figure I shows JFET parameter-geometry relationships.

GATE 1

L

Z

DRAIN

SOURCE

Th_{el}

2a

CHANNEL

GATE 2

SIMPLIFIED CROSS SECTION

FUNCTION OF:

L – CHANNEL LENGTH . . . . . . .PROCESS-QUALITY-DESIGN

Z – CHANNEL WIDTH . . . .''GEOMETRY'' DESIGN

2a – CHANNEL DEPTH . . . . . . .PRODUCTION-VARIABLE

Th_{el} – EPIT. DEPTH . . . . .PROCESS-QUALITY-DESIGN

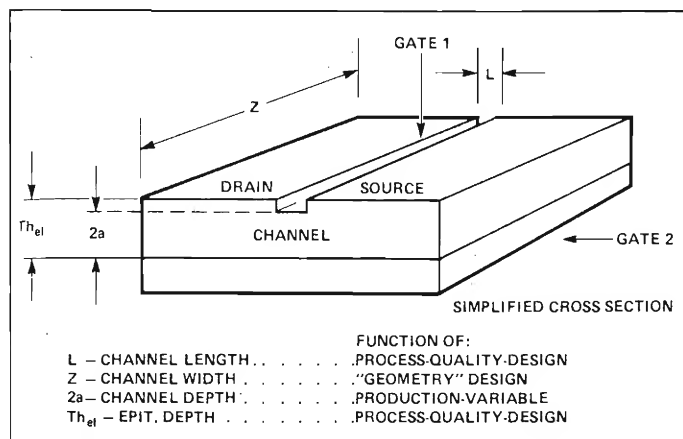



Fig. 1. FET Parameter-Geometry Relationship

	Increasing Dimension	L	Z	2a	Th_{EL}
Y_{fs}	Transadmittance	−	+	+	−
I_{DSS}	Max. Drain Current	−	+	+	−
$V_{GS(OFF)}$	Cut-Off Voltage	0	0	+	0
r_{DS}	On Resistance	+	−	−	+
C_{iss} C_{rss}	Gate Capacitance	+	+	0	+
I_{GSS}	Gate Leakage	+	+	0	0
e_n	Short Circuit Input Noise	=	−	−	+
i_n	Input Current Noise	+	+	0	0
Y_{OS}	Output Admittance	−	+	+	+
$V_{(BR)GSS}$	Breakdown Voltage	−	0	0	+

Choices

By design, key features such as $r_{DS} < 5$ ohms, $BV_{DGO} > 300$ V, $C_{iss} < 2$ pF can be designed individually into various FETs. Teledyne selection guides can quickly help you narrow your choice for a particular application, and eliminate problem parameters.

Low Noise FETs – A Challenge to Low Noise Bi-Polars

Introduction

Field Effect Transistors were traditionally used in applications requiring high source impedances.

For low noise applications, the "rule of thumb" has been to use a FET when source impedances ⩾ 100k ohms are necessary.

Times have changed and now the designer must re-evaluate how FET versus bi-polar transistor amplifiers compare. A close scrutiny of bi-polar and FET specifications, along with circuit breadboarding, will startle most designers. Currently available junction N-Channel FETs, such as the 2N5391-6 and 2N4867-9, exhibit noise figures equivalent to the best bi-polar transistors with source impedances less than 10k ohms — with no compromise in other desirable FET features.

This paper reviews the important noise areas including:

1. Important considerations in the determination of noise figure.
2. Basic definitions.
3. Simplified test procedures.
4. The use of Equivalent Noise and Current Sources.
5. Comparative performance of the low noise FET versus bi-polar transistors.
   a. Low frequency considerations.
   b. Source impedance considerations.
   c. Other FET advantages.

Types of Noise

Thermal noise, excess noise, and shot noise are three of the more important types of noise phenomena inherent in both bi-polar and FET transistors.

1. Thermal Noise is characterized by a condition of thermodynamic equilibrium; that is, at any specific temperature the associated noise power of a transducer with a specified noise bandwidth equals the product of 4 x Boltzmann's constant (k), absolute temperature in degrees Kelvin, and the noise bandwidth (B) in hertz.
2. Excess Noise in semiconductors results from random fluctuations in conductivity and surface effects. The spectral density of excess noise varies with the reciprocal of frequency and is usually referred to as the "l/f" noise. Negligible in low noise FETs, this "l/f" noise increases approximately 3dB per octave below a certain frequency in bi-polars, often 100 Hz.
3. Shot Noise is associated with the flow of dc currents and is negligible above 1 kHz for most semiconductors.

Accurate Noise Figure Measurements

Many methods of noise figure measurements are used in the industry. The commercially available Quan Tech 2236 Control and 2237 Filter Unit is a flexible piece of equipment useful for all but a few exotic requirements. Jury-rigged equipment will work equally well, although it is slower for quantity testing. Three of the common methods in use are:

1. CW-Signal Generator Method — Utilizes a calibrated signal generator and a true RMS power meter to determine the frequency dependency of transducer gain and the transducer noise bandwidth. From this informa-

tion, the output noise resulting from the input termination and the noise factor of the transducer can be determined. This is the most commonly used method.

2. Dispersed-Signal Method — Utilizes a calibrated white noise source such as a noise diode and a precision attenuator. By switching the attenuator in and out, the output noise can be separated into that generated by the transducer and that generated by the noise source.

3. Comparison Method — Compares the transducer under test and a standard transducer of the same type with a known noise factor. This method is satisfactory for go/no-go testing provided an accurate reference unit is obtained through a more precise method.

Noise figure is defined as the ratio of the signal-to-noise power ratio at the input to that at the output. It varies as a function of the input impedance, frequency, and operating current level. Measurement difficulty is encountered in determining low noise figure values accurately, particularly with source impedances greater than 100k ohm. With 100k ohm source impedance, the 2N5391-6 devices contribute little noise compared to the source impedance noise.

Equivalent Noise Voltages — Voltage (e_n), Current (i_n)

A more meaningful and useful method of Bi-Polar and Field Effect Transistor noise figure measurements is to convert "e_n" and "i_n" measurements to noise figure in dB as a function of a specified source resistance. In any active device, junction-transistor or FET, there is a certain amount of noise "e_n" (referred to the input) that is independent of source impedance. There is another noise component, "i_n", whose effect is directly dependent on source impedance. "e_n" is the equivalent noise voltage for a one hertz bandwidth. "$\sqrt{e_n^2}$" represents the spectral density of the equivalent short-circuit noise voltage generator at the input of the FET at a specified frequency and bandwidth. The equivalent input noise voltage is determined by measuring the device noise output with the input ac shorted. Input referred noise is the output voltage divided by the circuit gain. For practical measurement purposes, Rg = 100 ohms is a sufficient input ac short as illustrated in Figure 1. A similar procedure is used for bi-polars except base current is supplied to obtain the desired collector current.

1. Set signal generator for 100mV.
2. Then $V_{gs} = 0.1 \frac{(100\Omega)}{(10^6\Omega)} = 10^{-5} = 10\mu V$
3. Set total gain to 1000.
4. VTVM at output now reads 10mV.
5. Short out 100Ω resistor.
6. VTVM now reads 1mV for every microvolt of noise.

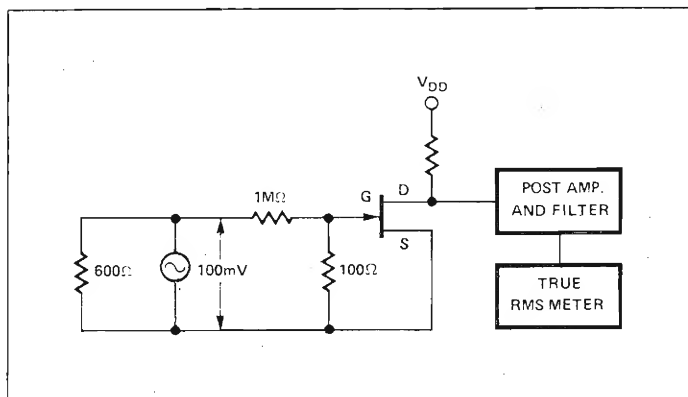



Fig. 1.

"i_n" is the equivalent noise current for a one hertz ba width. "$\sqrt{i_n^2}$" represents the spectral density of the equ lent open-circuit noise current generator at the input of transistor at a specified frequency and bandwidth. Eq alent input noise current is determined by dividing output noise (with the input ac open circuited) by the cuit gain and input ac impedance. For practical measu ment purposes, Rg = 1000MΩ is a sufficient input ac o as illustrated in Figure 2.

1. Set signal generator for 10mV with S1 in position
2. Set total gain to 10.
3. VTVM now reads 100 mV.
4. Switch S1 to position 2.
5. Meter reads one mV for each 10^{-13} A (0.1pA) of noi

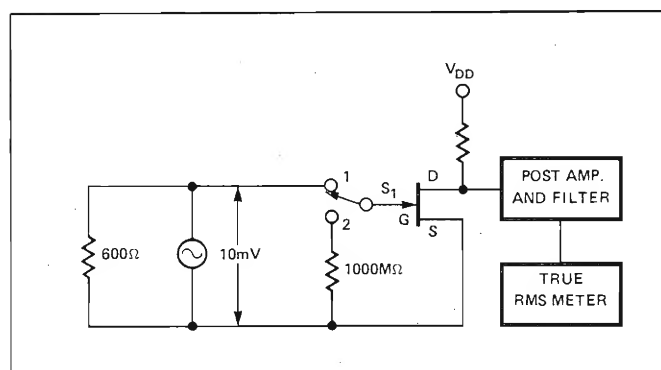



Fig. 2.

Noise voltage and current are functions of frequency. I FETs the former increases while the latter decreases wit decreasing frequency. The noise sources are relativel independent of drain current and drain-to-source voltage wich is unlike the strong dependence of the noise sourc on collector current in a transistor. The basic equivaler noise source circuit is shown in Figure 3.

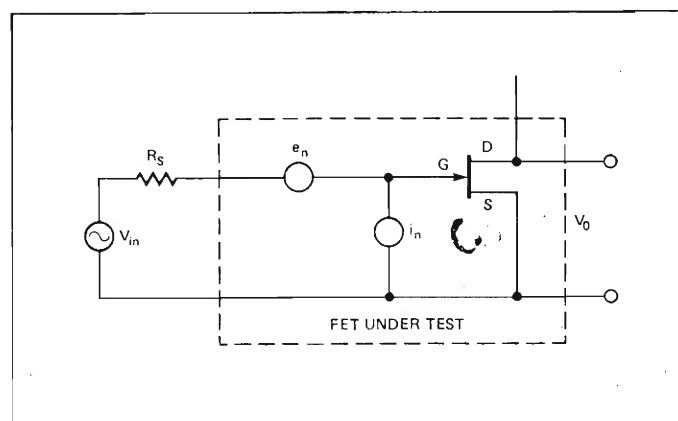



Fig. 3. Equivalent Noise Sources

Noise Figure Conversion From Equivalent Noise Sources

Device noise can be expressed in terms of power or voltage gains and, when expressed in dB noise figure, the two methods are the same.

In calculating noise figure from the equivalent noise sources, a correlation factor (γ) exists influencing the NF as expressed in equation (8). The correlation factor is the

result of the random nature of noise, specifically the instantaneous noise voltage and noise current peaking at different intervals (random period). γ may be treated like the cosine of the angle between e_n and i_nR_s. If the phase difference is zero, the cosine $< 0° = 1$. This is full correlation and $\gamma = 1$. If zero correlation is assumed, phase angle of noise current and voltage equals 90°, and $\gamma = 0$.

It is widely accepted through test results that $\gamma = 1$ is a closer approximation. The curves, nomograph, and future discussion is based on this approximation.

Noise figure may be expressed as:

$$Fo\ (dB) = 10 \log \frac{(V_I/N_I)^2}{(V_0/N_0)^2} = 20 \log \frac{V_I/N_I}{V_0/N_0}$$

where

V_I = Signal voltage into transducer.
N_I = Noise voltage into transducer.
V_0 = Signal voltage out of transducer.
N_0 = Noise voltage out of transducer.

For calculating the noise figure of an amplifier, the schematic in Figure 4 is useful.

V_S – INPUT SIGNAL VOLTAGE
e_nR_s – RESISTOR NOISE VOLTAGE
e_n – EQUIVALENT NOISE VOLTAGE
i_n – EQUIVALENT NOISE CURRENT
A – VOLTAGE AMPLIFICATION
γ – CORRELATION FACTOR

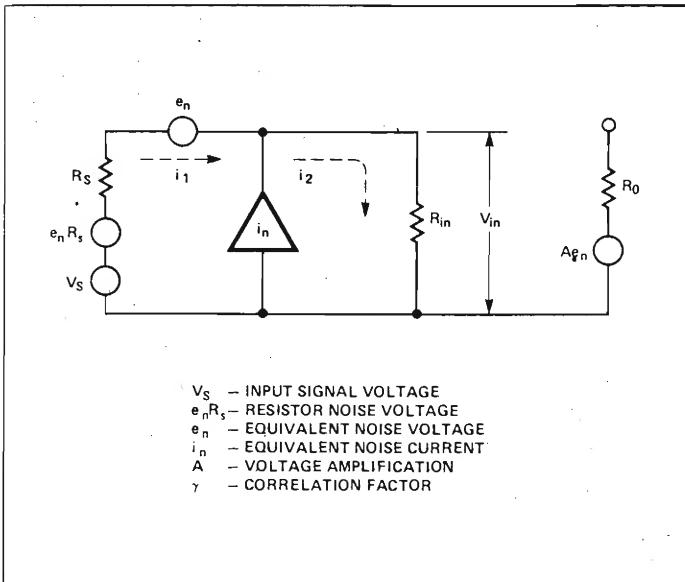



Fig. 4. Amplifier Equivalent Noise Circuit

Solving for the noise factor (multiple of noise voltage obtained, other than expected from device gain, as the source resistor noise passes through the device circuit) from the equivalent circuit.

$$F = \frac{v_{in}A}{A_v v_{nRs}} = \frac{i_2 A R_{in}}{A_v v_{nRs}} \qquad (1)$$

$$\text{where } A_v = Av_{in} = \frac{A R_{in}}{R_{in} + R_s}$$

Neglecting the v_s voltage source from Figure 4 which does not enter into the noise equation.

$$e_{nRs} + e_n - V_{in} = i_1 R_s \qquad (2)$$

$$V_{in} = i_2 R_{in} \qquad (3)$$

$$i_2 = i_1 + i_n \text{ or } i_1 = i_2 - i_n \qquad (4)$$

Substituting (3) & (4) into (2)

$$e_{nRs} + e_n - i_2 R_{in} = i_2 R_s - i_n R_s$$

Rearranging

$$\frac{e_{nRs} + e_n + i_n R_s}{R_s + R_{in}} = i_2 \qquad (5)$$

Substituting (5) into (1)

$$F = \frac{AR_{in}\,(e_{nRs} + e_n + i_n R_s)}{A_v e_{nRs}\,(R_s + R_{in})} \qquad (6)$$

Reducing the equation, adding the noise sources as the square root of the sum of the noise voltage squared and expressing in dB results in:

$$NF = 20 \log \left[\frac{e_n{}^2{}_{Rs} + (e_n + \gamma i_n R_s)^2}{e_n{}^2 R_s}\right]^{1/2} \qquad (7)$$

$$NF = 10 \log \left[1 + \frac{e_n{}^2 + i_n{}^2 R^2{}_s + 2\gamma e_n i_n R_s}{4KTR_s}\right] \qquad (8)$$

Where $e_n{}^2{}_{Rs} = 4KTR_s$ and
$K = 1.38 = 10^{-23}$ joules per degrees Kelvin
T = Absolute temperature in degrees Kelvin
B = Bandwidth

Now assume $\gamma = 1$ (Worst Case Noise Figure) and Bandwidth = 1 then:

$$NF = 10 \log \left[1 + \frac{(e_n + i_n R_s)^2}{4KTR_s}\right] \qquad (9)$$

Optimized Noise Figure

In designs where optimum noise is extremely important and the source resistance flexible, R_s should be chosen to give the lowest noise. Considering Equation 8 where $e_n = 10^{-9}$ volts and $i_n = 10^{-12}$ amperes, notice that at low source resistance e_n will be generally the predominant term while at high source resistance i_n is predominant.

The optimum source resistance for minimum noise figure can easily be obtained by taking the derivative of the terms in equation (8) with respect to R_s and setting it equal to zero.

$$\frac{dF}{dR_s} = 0 =$$

$$\frac{4KTR_s\,(2i_n{}^2R_s + 2\gamma e_n i_n) - (e_n{}^2 + i_n{}^2 R_s{}^2 + 2\gamma e_n i_n R_s)\,4KT}{(4KTR_s)^2} = 0$$

Reducing and subtracting terms

$$i_n{}^2 R_s{}^2 = e_n{}^2$$

$$R_s = \frac{e_n}{i_n} \qquad \text{For } NF_{min} \qquad (10)$$

Notice for the bi-polar transistor "i_n" (from Figure 6 & 7) that a typical optimum source resistance is 10k @ 10μA.

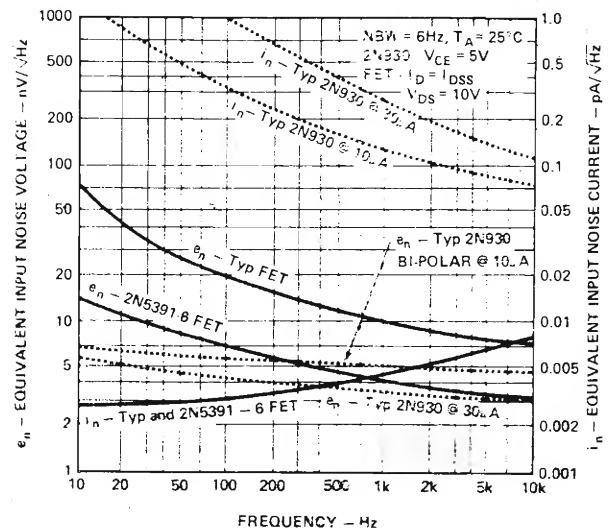



Fig. 5. Equivalent Input Noise Voltage and Current vs. Frequency

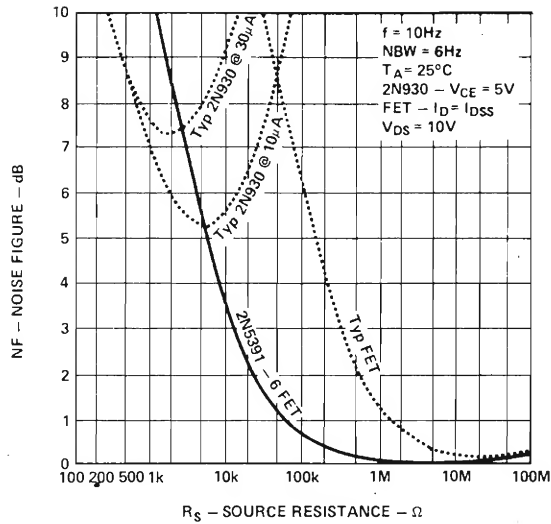



Fig. 6. Noise Figure vs. Source Resistance

Fig. 8. Equivalent Input Noise Current vs. Current

Fig. 7. Noise Figure vs. Source Resistance

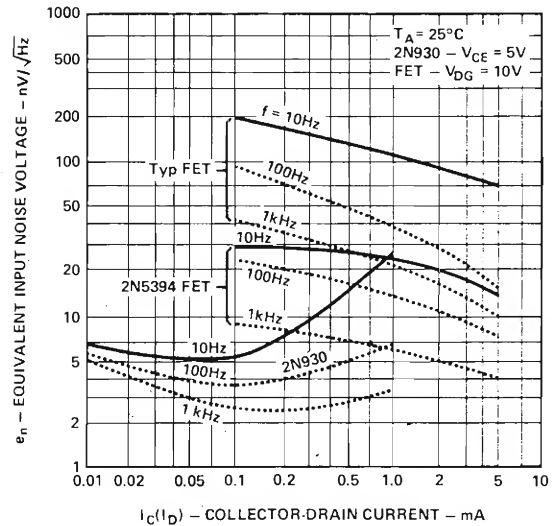



Fig. 9. Equivalent Input Noise Voltage vs. Current

The 2N5391-6 field effect transistor optimum source resistance is 1 to 10M. However, even at the optimum source resistance for a typical 2N930 type bi-polar transistor, the noise figure is higher than the 2N5391-6 series FET's.

Substituting equation (10) into (8) gives

$$NF_{min} = 10 \log \left[1 + \frac{(e_n + \gamma e_n)\, 2\, i_n}{4KT}\right] \qquad (11)$$

Assuming worst case $\gamma = 1$,

$$NF_{min} = 10 \log \left[1 + \frac{e_n i_n}{KT}\right]$$

Bi-Polar Versus FET Noise Comparison

The significant difference between the bi-polar and FET is in the "e_n" and "i_n" values as plotted in Figure 5, 8, and 9. Bi-polars are extremely sensitive to collector current variations and the circuit designer must beware. FET's are relatively insensitive to drain current variations, particularly "i_n". Notice that the FET "i_n" is 2-3 orders of magnitude lower than the bi-polar.

FET devices perform particularly well at low frequencies (<100Hz) i.e., they do not show a significant l/f noise slope. Naturally at low frequencies, the noise figure drops rapidly as source resistance increases.

Most impressive about the FET, particularly the 2N5391-6 series, is its low noise over many decades of source resistance value. This flexibility is advantageous in strain-gauges, light sensors, thermistors, and other transducers. Designers of standard amplifier circuits who will be using varying source resistance might well use the 2N5391-6 or 2N4867-9 series FET's to provide the low noise flexibility.

If low noise applications restrict source resistances to less than 500 ohms, the bi-polar will probably continue to be the best.

Noise Figure Nomograph

The Noise Nomograph is a useful method of solving the various noise equations when it is assumed that the correlation factor (γ) is unity, a close approximation for most devices.

The more important noise equations are:

$$NF = 10 \log \left[1 + \frac{(e_n + i_n R_s)^2}{4KTRg}\right] \qquad (1)$$

$$NF_{min} = 10 \log \left[1 + \frac{e_n i_n}{KT}\right] \qquad (2)$$

$$R_{opt} = \frac{e_n}{i_n} \qquad (3)$$

Example using the nomograph:

Choose between using a 2N5391-6 series FET and a 2N930 bi-polar transistor in a low noise amplifier with 30k ohm input impedance where 10Hz noise is critical.

2N930 ($I_C = 10\mu A$) $e_n = 7nV/\sqrt{Hz}$

$I_n = 1.5pA/\sqrt{Hz}$

2N5391-6 Series FET $e_n = 14nV/\sqrt{Hz}$ i_n

$= .0028pA/\sqrt{Hz}$

Solution

A. Determine 2N930 Noise Figure

1. Connect "A" e_n ($7nV/\sqrt{Hz}$) and "B" i_n ($1.5pA/\sqrt{Hz}$) points with a straight line to "C", $NF_{min} = 5.1$ dB.
2. Connect "E" ($R_g = 30k\Omega$) and "D" ($R_{opt} = 5k\Omega$) points with a straight line to "F" ($R_g/R_{opt} = 6$).
3. Transfer "F" to "G" on $\frac{R_{opt}}{R_g}$, $\frac{R_g}{R_{opt}}$ scale and connect points "C" & "G" with a straight line.
4. Determine the intersection of this line and the NF scale "H" – read 7.5 dB noise Figure.

B. Determine 2N5391-6 Series Noise Figure

1. Connect "J" e_n ($14nV/\sqrt{Hz}$) and "K" i_n ($.0028pA/\sqrt{Hz}$) points with a straight line to "L", $NF_{min} = 0.04$ dB.
2. Connect "E" ($R_g = 30k\Omega$) and "M" ($R_{opt} = 5M\Omega$) points with a straight line to "N" ($R_{opt}/R_g = 160$).
3. Transfer "N" to "O" on R_{opt}/R_g, R_g/R_{opt} scale and connect points "L" and "O" with a straight line.
4. Determine the intersection of this line and the NF scale "P" – read 1.6 dB noise figure.

C. From the above solutions using the Noise Nomograph the 2N5391-6 series FET's would have the lower noise by 5.9 dB and be the much better choice.

NOISE NOMOGRAPH

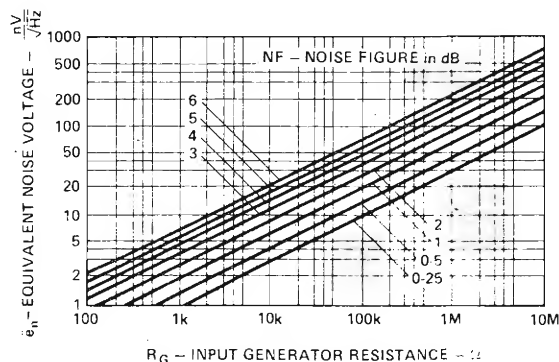
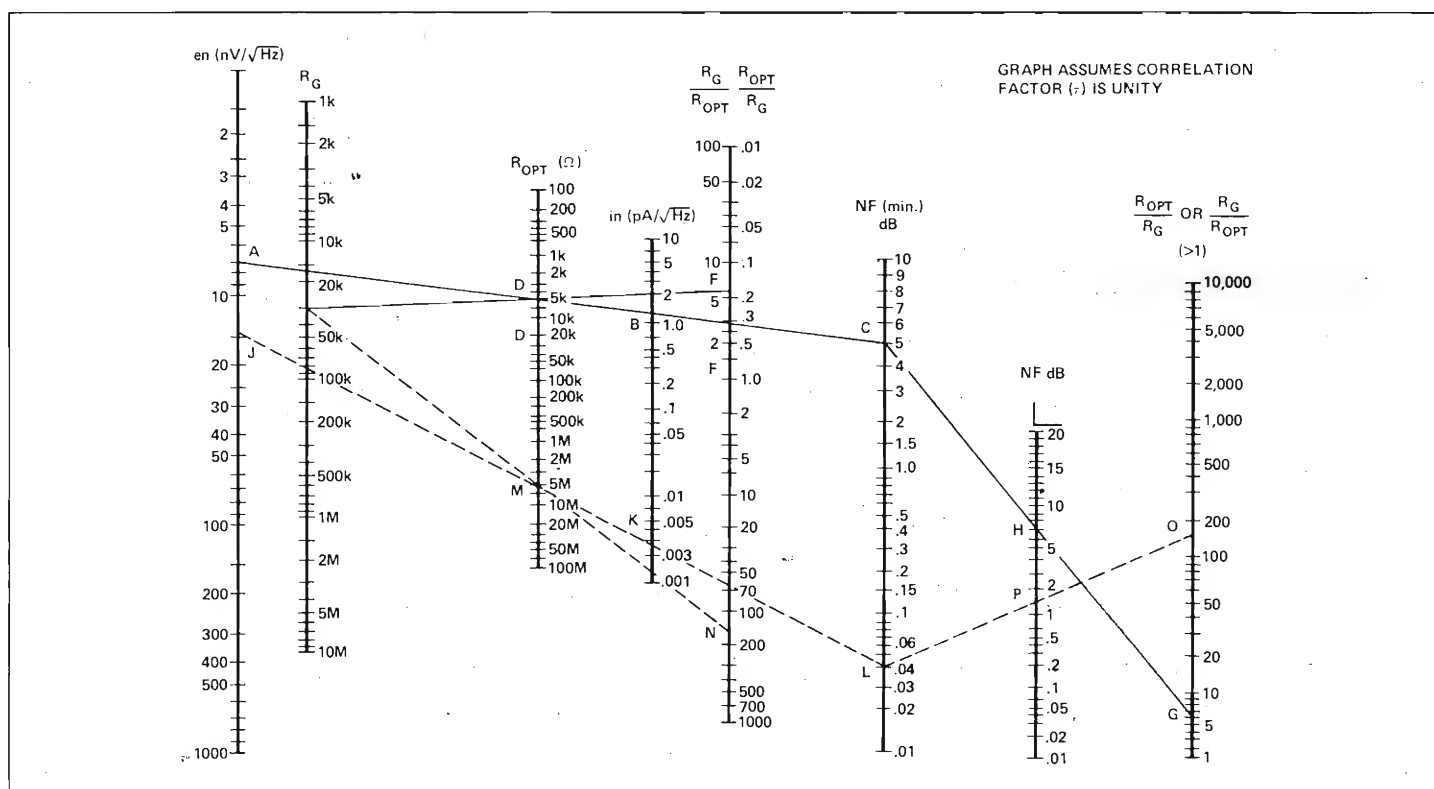



Fig. 10. Noise Figure—Noise Voltage Conversion Chart

Noise Voltage Conversion Chart

Practically all junction FETs being manufactured today have e_n sufficiently low that it can be neglected for Generator Resistance values up to 10 Megohms. On this basis the simplified approximate chart can be used as given in Figure 10.

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3. EIA Standard RS-354, "The Measurement of Transistor Equivalent Noise Voltage and Equivalent Noise Current at Frequencies up to 20kHz," April, 1968.
4. EIA Standard RS-353, "The Measurement of Transistor Noise Figure at Frequencies up to 20kHz by Sinusoidal Signal-Generator Method," April 1968.
5. Teledyne Semiconductor, "Field Effect Transistors – Theory and Application," Technical Bulletin No. 1, May 1971.

FET Small-Signal Analysis

Analysis of low-frequency, small-signal field-effect transistor amplifier stages can be accomplished with practical accuracy by using simple equations. The techniques described here provide general coverage of operation slightly over 100 kHz. If capacitance effects are included, the equations will be useful into the megahertz region.

Common-Source Amplifier

The schematic for a common-source amplifier and its equivalent circuit is shown in Fig. 1. Capacitance has been omitted and is neglected in the derivation that follows. Also, if it is assumed that negligible current flows into R_g, then

$$\frac{1}{g_{gs}} + R_g >> R_L \text{ or } R_S$$

Voltage Gain

Referring to the equivalent circuit (Fig. 1),

$$A_V = -\frac{A}{1 + A\beta}$$

where and

$$-A = \frac{e_o}{E_{gs}} \qquad A\beta = \frac{V_{RS}}{E_{gs}}$$

Solving for the output current

$$I_o = g_m E_{gs} \left(\frac{\frac{1}{g_o}}{\frac{1}{g_o} + R_L + R_S} \right) =$$

$$g_m E_{gs} \left[\frac{1}{1 + g_o (R_L + R_S)} \right]$$

Since

$$-A = -\frac{I_o R_L}{E_{gs}}$$

Fig.1. FET common-source amplifier schematic and equivalent circuit.

then

$$-A = \frac{-g_m R_L}{1 + g_o (R_L + R_S)}$$

Also

$$A\beta = \frac{I_o R_S}{E_{gs}} = \frac{g_m R_S}{1 + g_o (R_L + R_S)}$$

and

$$A_V = \frac{\dfrac{-g_m R_L}{1 + g_o (R_L + R_S)}}{1 + \dfrac{g_m R_S}{1 + g_o (R_L + R_S)}}$$

$$A_V = \frac{-g_m R_L}{1 + g_o (R_L + R_S) + g_m R_S}$$

However, if $g_o (R_L + R_S) << 1$, then

$$A_V \approx \frac{-R_L}{\frac{1}{g_m} + R_S}$$

Input Impedance

The total input impedance (Z_{int}) is equal to R_g in parallel with the impedance (Z_{in}) seen at the gate terminal.

Solving for the gate terminal impedance,

$$Z_{in} = \frac{\frac{1}{g_{gs}}}{1 - A_{VS}}$$

where A_{VS} (gate to source voltage gain) $= V_{RS}/E_{in}$. However, since $V_{RS} = E_{in} - E_{gs}$ and

$$E_{gs} = \frac{V_{RS}}{A\beta} = \frac{\frac{V_{RS}}{g_m R_S}}{1 + g_o R_L + g_o R_S}$$

then

$$V_{RS} = E_{in} - \frac{\frac{V_{RS}}{g_m R_S}}{1 + g_o R_L + g_o R_S}$$

$$V_{RS} = \frac{E_{in} g_m R_S}{1 + g_o (R_L + R_S) + g_m R_S}$$

and

$$A_{VS} = \frac{V_{RS}}{E_{in}} = \frac{g_m R_S}{1 + g_o (R_L + R_S) + g_m R_S}$$

Therefore,

$$Z_{in} = \frac{\frac{1}{g_{gs}}}{1 - \dfrac{g_m R_S}{1 + g_o (R_L + R_S) + g_m R_S}}$$

and

$$Z_{int} = R_g \parallel \frac{\frac{1}{g_{gs}}}{1 - \dfrac{g_m R_S}{1 + g_o (R_L + R_S) + g_m R_S}}$$

Bootstrapping

The impedance R_g is often the limiting factor when trying to obtain the highest possible input impedance. To increase the effective impedance of R_g, a bootstrapping technique can be employed as shown in Fig. 2.

For this circuit,

$$Z_{int} = \frac{R'_g}{1 - A_{VS}} \parallel \frac{\frac{1}{g_{gs}}}{1 - A_{VS}}$$

Fig. 2. Schematic and equivalent circuits of FET bootstrapping technique.

and with R_b in parallel with R_S, the A_{VS} equation derived previously is modified to

$$A_{VS} = \frac{g_m\left(\frac{R_S R_b}{R_S + R_b}\right)}{1 + (g_m + g_o)\frac{R_S R_b}{R_S + R_b} + g_o R_L}$$

Note that for the Z_{int} equation A_{VS} being less than unity raises both impedance factors to be paralleled.

The effect of A_{VS} on g_{gs} also applies to the gate-to-source capacitance.

$$C_{gs} \text{ equivalent} = C_{gs}(1 - A_{VS})$$

The gate-to-drain capacitance C_{gd} must be considered with due appreciation for the Miller effect. The Miller effect is simply an apparent multiplication of the capacitance.

$$C_{gd} \text{ equivalent} = C_{gd}(1 + |A_V|)$$

where $|A_V|$ is the absolute value of the gate-to-drain voltage gain.

The most significant effect on circuit performance is caused by C_{gd} and by comparison, C_{gs} generally can be neglected. For this reason many specification sheets do not list the value of C_{gs}.

Output Impedance

The total output impedance (Z_{OT}) is equal to $R_L \| Z_o$ where Z_o is the impedance looking into the drain terminal. To determine the values of Z_o, first find the change in output voltage resulting from a Δ shift in R_L. Two equations evolve depending on whether $1/g_o$ is finite (ΔE_{0I}) or $1/g_o$ is infinite (ΔE_o).

$$\Delta E_{0I} \approx \frac{-E_{in} g_m}{1 + g_o(R_L + R_S) + g_m R_S} \Delta R_L$$

when $1/g_o$ is finite, and

$$\Delta E_o \approx \frac{-E_{in} g_m}{1 + g_m R_S} \Delta R_L$$

when $1/g_o$ is infinite.

The per unit difference in these equations is a measure of the output impedance relative to R_L.

$$\frac{\Delta E_o - \Delta E_{0I}}{\Delta E_{0I}} = \frac{\frac{-E_{in} g_m \Delta R_L}{1 + g_m R_S} + \frac{E_{in} g_m \Delta R_L}{1 + g_o(R_L + R_S) + g_m R_S}}{\frac{E_{in} g_m \Delta R_L}{1 + g_o(R_L + R_S) + g_m R_S}}$$

$$\frac{\Delta E_o - \Delta E_{0I}}{\Delta E_{0I}} = \frac{g_o(R_L + R_S)}{1 + g_m R_S}$$

From the equivalent circuits of Fig. 3 calculate Z_o from $\frac{\Delta E_o - \Delta E_{0I}}{\Delta E_{0I}}$ as follows:

$$\frac{\Delta E_o - \Delta E_{0I}}{\Delta E_{0I}} = \frac{g_m E_{gs} R_L - g_m E_{gs}\left(\frac{Z_o R_L}{Z_o + R_L}\right)}{g_m E_{gs}\left(\frac{Z_o R_L}{Z_o + R_L}\right)} \approx \frac{R_L}{Z_o}$$

and

$$Z_o = \frac{R_L}{\frac{\Delta E_o - \Delta E_{0I}}{\Delta E_{0I}}} = \frac{1 + g_m R_S}{g_o(R_L + R_S)}(R_L)$$

If there had been no source resistance R_S, the device output impedance would have been $1/g_o$ as indicated by the equivalent circuit (Fig. 1). The effect of the local degeneration resistor R_S has reduced the output admittance to

$$\left[\frac{g_o}{1 + g_m R_S}\right]\left[\frac{R_L + R_S}{R_L}\right]$$
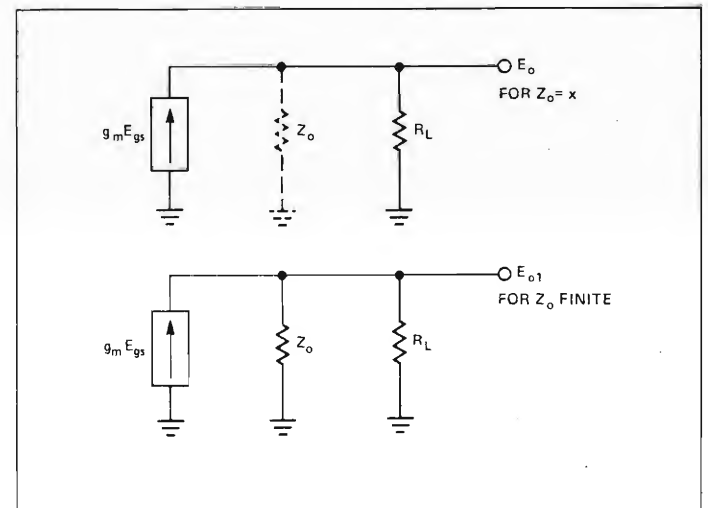
Fig. 3. Common-source output circuits for E_o when $Z_o = \infty$ and E_{oI} when Z_o is finite.

The total output impedance now becomes

$$Z_{OT} = \frac{R_L\left(\frac{1 + g_m R_S}{g_o}\right)\left(\frac{R_L}{R_L + R_S}\right)}{R_L + \left(\frac{1 + g_m R_S}{g_o}\right)\left(\frac{R_L}{R_L + R_S}\right)}$$

$$Z_{OT} = \frac{R_L \dfrac{1 + g_m R_S}{g_o}}{R_L + R_S + \dfrac{1 + g_m R_S}{g_o}}$$

SOURCE FOLLOWER CIRCUIT

The schematic for a source follower circuit is shown in Fig. 4.
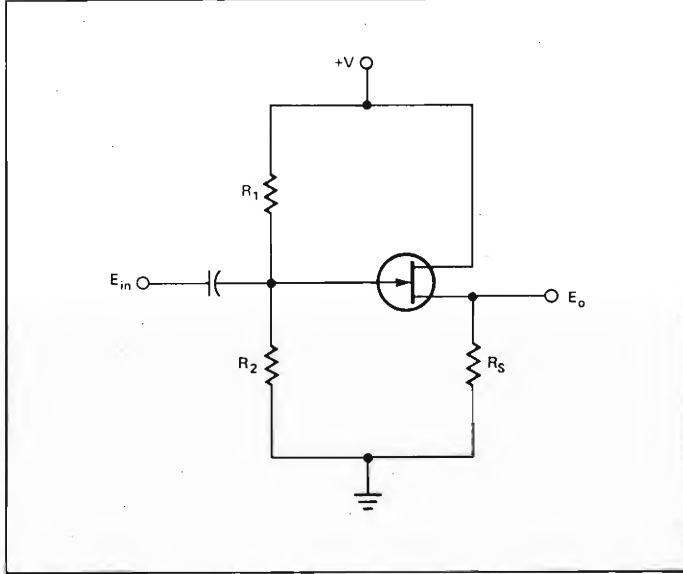
Fig. 4. Schematic of FET source follower circuit.

Voltage Gain

The same argument that was used to calculate A_{VS} for the common-source amplifier can be used to calculate the voltage gain for the source follower but with R_L equal to zero. Thus,

$$A_{VS} = \frac{g_m R_S}{1 + R_S (g_m + g_o)}$$

Input Impedance

$Z_{int} = R_g \,||\, Z_{in}$ where $R_g = R_1 \,||\, R_2$,

$$Z_{in} = \frac{\dfrac{1}{g_{gs}}}{1 - \dfrac{g_m R_S}{1 + R_S (g_m + g_o)}}$$

and

$$Z_{int} = R_g \left\| \frac{\dfrac{1}{g_{gs}}}{1 - A_{VS}} \right.$$

Output Impedance

The total output impedance $Z_{OT} = R_S \,||\, Z_o$. Z_o can be derived from the basic gain equation as follows:

$$A_V = \frac{g_m R_S}{1 + R_S (g_m + g_o)} = \frac{R_S}{\dfrac{1}{g_m} + R_S \dfrac{g_o}{g_m} + R_S} = \frac{E_{out}}{E_{in}}$$

The above equation is in the form of a voltage divider as shown in Fig. 5. Thus it can be seen that the FET output impedance (Z_o) is

$$Z_o = \frac{1}{g_m} + R_S \frac{g_o}{g_m}$$

The total output impedance Z_{OT} is

$$Z_{OT} = \frac{\dfrac{R_S}{g_m} + \dfrac{g_o}{g_m} R_S^2}{\dfrac{1}{g_m} + R_S \dfrac{g_o}{g_m} + R_S} = \frac{R_S + g_o R_S^2}{1 + R_S (g_o + g_m)}$$

As $g_o \to 0$, $Z_{OT} \to \dfrac{R_S}{1 + R_S g_m} = R_S \,||\, \dfrac{1}{g_m}$
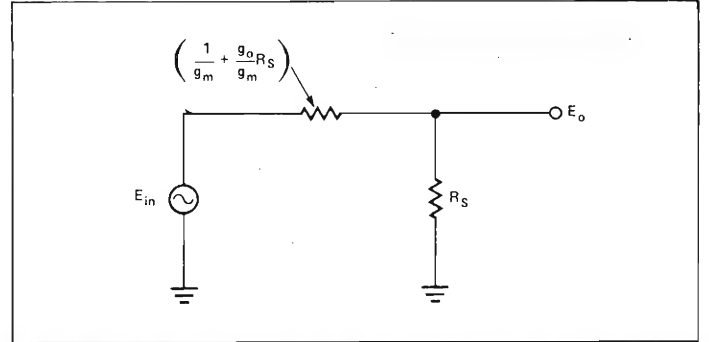
Fig. 5. Voltage divider equivalent of source follower output circuit.

COMMON-GATE AMPLIFIER

The common-gate amplifier and its equivalent circuit are shown in Fig. 6. This circuit is not mentioned in most literature but is important primarily in the analysis of feedback amplifiers.
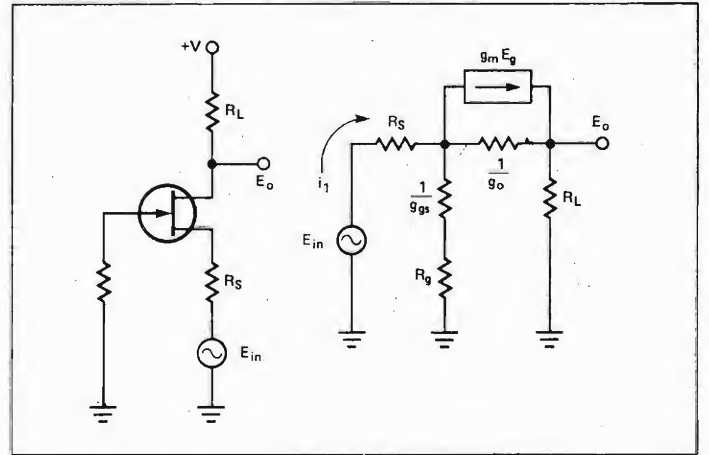
Fig. 6. Schematic and equivalent circuit of FET common-gate amplifier.

Voltage Gain

The gain equation is identical to that for the common-source amplifier except that no phase inversion occurs.

$$A_V = \frac{g_m R_L}{1 + g_o (R_L + R_S) + g_m R_S}$$

Input Impedance

Referring to the equivalent circuit Fig. 6, the current flow in the $1/g_{gs}$ branch is neglected (i.e., $1/g_{gs} + R_g >> R_L + 1/g_o + R_S$).

$$E_{in} = i_1 \left(R_S + \frac{1}{g_o} + R_L\right) - g_m E_g \frac{1}{g_o}$$

and

$$E_g = E_{in} - i_1 R_S$$

Substituting

$$E_{in} = i_1 \left(R_S + \frac{1}{g_o} + R_L\right) - E_{in} \frac{g_m}{g_o} + i_1 R_S \frac{g_m}{g_o}$$

$$E_{in}\left(1 + \frac{g_m}{g_o}\right) = i_1 \left(R_S + \frac{1}{g_o} + R_L + R_S \frac{g_m}{g_o}\right)$$

$$\frac{E_{in}}{i_1} = Z_{in} = \frac{R_S + \frac{1}{g_o} + R_L + R_S\frac{g_m}{g_o}}{1 + \frac{g_m}{g_o}}$$

$$Z_{in} = \frac{1}{g_o + g_m} + (R_S + R_L)\frac{g_o}{g_o + g_m} + \frac{R_S\, g_m}{g_o + g_m}$$

f $g_o << g_m$

then $Z_{in} \approx \frac{1}{g_m} + (R_S + R_L)\frac{g_o}{g_m} + R_S$

And if $(R_S + R_L)\, g_o << 1/g_m$, then $Z_{in} = 1/g_m + R_S$ where $1/g_m$ is a dynamic impedance seen looking into the source terminal of the FET.

Output Impedance

The output impedance is identical to that of the common-source stage.

SUMMARY

If the assumptions listed below are valid for the circuit in question, then the simplified equations in the chart may be used.

(a) $g_o(R_L + R_S) << 1$
(b) $g_o(R_L + R_S) << 1/g_m$
(c) $1/g_o >> R_L$
(d) $R_1||R_2 >> g_{gs}$
(e) Low-frequency capacitive reactances are negligible.

PARAMETER	COMMON SOURCE	SOURCE FOLLOWER	COMMON GATE
VOLTAGE GAIN	$A_v \approx \frac{-R_L}{\frac{1}{g_m} + R_S}$	$A_{VS} \approx \frac{R_S}{\frac{1}{g_m} + R_S}$	$A_v \approx \frac{R_L}{\frac{1}{g_m} + R_S}$
INPUT IMPEDANCE	$Z_{in} \approx R_1\|\|R_2$	$Z_{in} \approx R_1\|\|R_2$	$Z_{in} \approx R_S + \frac{1}{g_m}$
OUTPUT IMPEDANCE	$Z_o \approx R_L$	$Z_{oT} \approx R_S \|\| \frac{1}{g_m}$	$Z_o \approx R_L$

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Transadmittance Analysis

When trying to maximize voltage gain in FET amplifier circuits, the type with highest minimum guaranteed transadmittance, Y_{fs}, may seem desirable. It is not obvious that a Y_{fs} of 1000 μmhos may out-perform a device with a Y_{fs} of 5000 μmhos, but it is possible.

CONSIDERATIONS

There are three major considerations in designing even a simple audio amplifier — voltage gain, distortion, and noise figure. In various applications, each takes on varying importance and the normal compromises are made. Trade-offs are illustrated in the simple grounded source amplifier as shown in Fig. 1.

The best fixed operation would come from Fig. 1c where the current source is another FET or bi-polar current source arrangement. (See Fig. 2, R_S = line.) Each of the different arrangements is shown using the 2N4416 (U1994E) family curve as a vehicle. For example, using the extremes of the 2N4416 I_{DSS} = 5-15 mA with Fig. 1b R_S = 5K, then I_D operating current would vary from approximately 2 mA-5 mA. Each of the different modes is represented in Fig. 2.

VOLTAGE GAIN CONSIDERATION

Using any one of the arrangements in Fig. 1, the familiar voltage gain expression for low frequencies (C_{iss}, C_{rss} negligible) is:

(Eq. 1) $$A_V = \frac{-Y_{fs}R_L}{1 + R_L Y_{os}}$$

Now the question arises, how does the change in Y_{os} with voltage, Y_{fs} with current, the magnitude of R_L, and the interaction of R_L and Y_{os} all fit together to maximize voltage gain?

Using the basic drain current and transadmittance equations

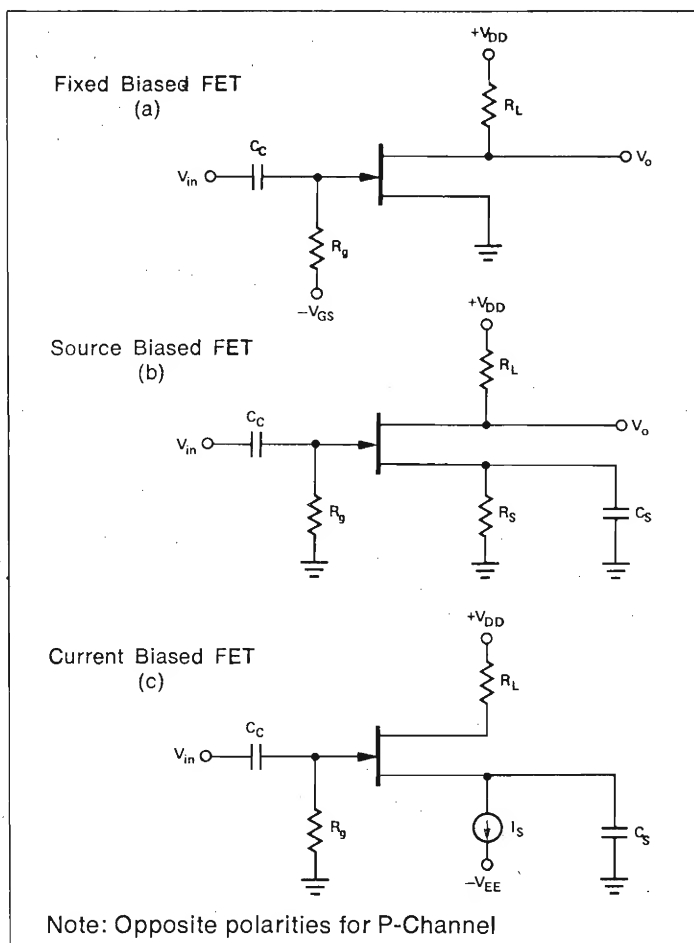



Fig. 1. N-Channel FET Bias Configurations

Note: Opposite polarities for P-Channel

(Eq. 2) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$ & $Y_{fs} = Y_{fso}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)$

where $Y_{fso} \doteq \frac{2\, I_{DSS}}{V_{GS(OFF)}}$

Substituting these equations into the general voltage gain expression, we obtain

(Eq. 3) $A_V = \frac{-2(V_{DD} - V_{DGnd})}{V_{GS(OFF)} - V_{GS}}$ and $A_{V(min)} = -\frac{2\,(V_{DD} - V_{DGnd})}{V_{GS(OFF)}}$

The $A_{V(min)}$ equation really becomes a device figure of merit when unlimited supply voltage is available by substituting $V_{(BR)GSS}$ for $V_{DD} - V_{DGnd}$. This is fine but in most cases, a finite V_{DD} supply is available. Practically speaking the minimum voltage that can operate V_{DG} (not V_{DS}) in a device is the device $V_{GS(OFF)}$, but preferably $V_{GS(OFF)} + 2$ V. If we use the preferable voltage minimum, then:

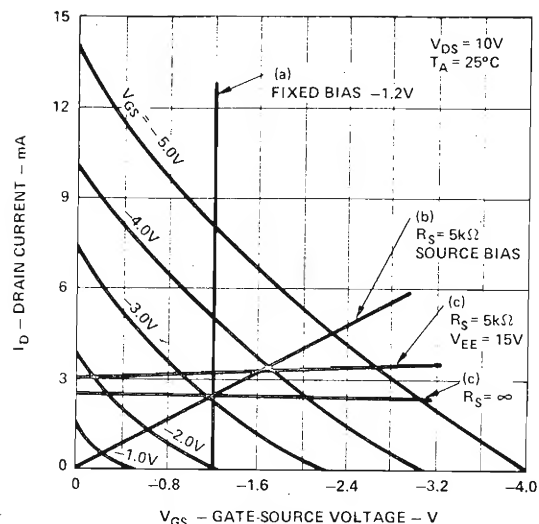



Fig. 2. FET Bias Operating Conditions

(Eq. 4) $R_L = \frac{V_{DD} - V_{GS(OFF)} - 2}{I_D}$

VOLTAGE GAIN EXAMPLE

Again using the curves applicable to the 2N4416 (U1994E) and its derivatives such as the 2N4302, a table and graph can be constructed to analyze Fig. 1c in conjunction with Equation 1 and 4. Assume $V_{DD} = +15$ V, $V_{EE} = -15$ V, and $R_S = \infty$ bypassed current source. Ambient temperature 25°C.

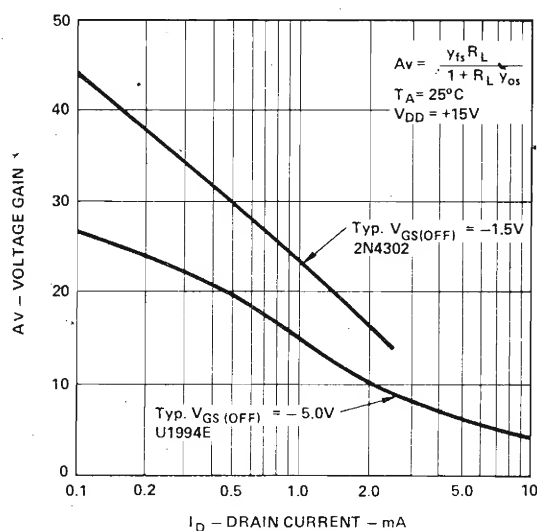



Fig. 3. Comparative Voltage Gains

Test	Units	$V_{GS} = 0$	I_D Value 2.5 mA	1 mA	0.5 mA	0.2 mA	0.1 mA	Device* No.
Y_{fs}	μmhos	3500 5500	3500 3350	2800 2500	2050 1800	1200 1100	675 575	A B
Y_{os}	μmhos	35 90	35 50	27 40	20 30	13 20	7 10	A B
R_L	Kohms	4.6K 0.57K	4.6K 3.2K	11.5K 8K	23K 16K	57.5K 40K	115K 80K	A B
Calculated Voltage Gain A_V		13.8 3.0	13.8 9.2	24.0 15.2	28.5 19.5	39.0 24.4	43.0 25.5	A B

*A – $V_{GS(OFF)} = -1.5$ V, $I_{DSS} = 2.5$ mA   B – $V_{GS(OFF)} = -5.0$ V, $I_{DSS} = 14$ mA

From Fig. 3 one can conclude that strictly on a voltage gain basis, it is better to select a lower I_{DSS}, $V_{GS(OFF)}$ unit such as the 2N4302, 2N4220 instead of units featuring higher Y_{fs} minimum such as the 2N4416, U1994E combination. As will be discussed, this is completely valid when input signal swings are only a few millivolts.

DISTORTION CONSIDERATIONS

The FET, unlike other semiconductor devices and vacuum tubes, follows the square law curve closely. Thus, li e beyond the second harmonic is present with any incoming sine wave. By combining the DC and AC components of gate-source voltage in Equation 2, harmonic distortion can be determined.

By definition:

$$\text{(Eq. 5)} \quad D_H(\%) = \frac{V_{rms} \text{ of 2nd harmonic}}{V_{rms} \text{ of fundamental}} \times 100 = \frac{V_{in(peak)}(100)}{V_{GS\ op} - V_{GS(OFF)})}$$

In this case, the higher $V_{GS(OFF)}$ device operated further away from cutoff (near $V_{GS} = 0$ — more linear portion of the transfer curve — Fig. 2), will reduce distortion. Likewise the harmonic distortion is directly proportional to the peak input signal. If only a few millivolts, the device $V_{GS(OFF)}$ has a negligible effect on distortion.

Typical input signals usually consist of complex waveforms of several frequencies, resulting in intermodulation distortion from the harmonics present. By combining the DC and AC components of gate-source voltage, by definition:

$$D_{IM} = \frac{V_{rms} \text{ of intermodulation components}}{V_{rms} \text{ of fundamental}} \times 100 = \frac{V_{in1} \cdot V_{in2}(100)}{1.4(V_{GS\ op} - V_{GS(OFF)}\ V_{in1}^2 + V_{in2}^2}$$

Just as for D_H, Equation 5, intermodulation distortion is minimal for operation near $V_{GS\ op} = 0$ and for higher $V_{GS(OFF)}$ devices, although slight. The amplitude of the input signals is most significant.

HARMONIC DISTORTION EXAMPLE

A similar table and graph using Eq. 5 can be constructed for the same type of devices as for voltage gain.

From Fig. 4 one can conclude that for 100 mVpk, there is a negligible difference in harmonic distortion over a wide range of device $V_{GS(OFF)}$ and operating current. At higher levels, the difference becomes significant. The same type of curves would be generated for intermodulation distortion.

To reduce distortion, at the expense of voltage gain, feedback such as an unbypassed source resistor, R_S, can be used. In this case, distortion is reduced by the product of $(1 + Y_{fs}R_S)$. For calculations, this term is added to the denominator of both Eq. 5 and 6.

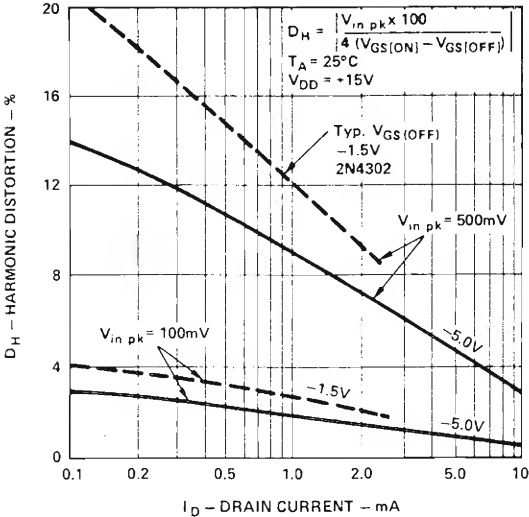



Fig. 4. Comparative Harmonic Distortion

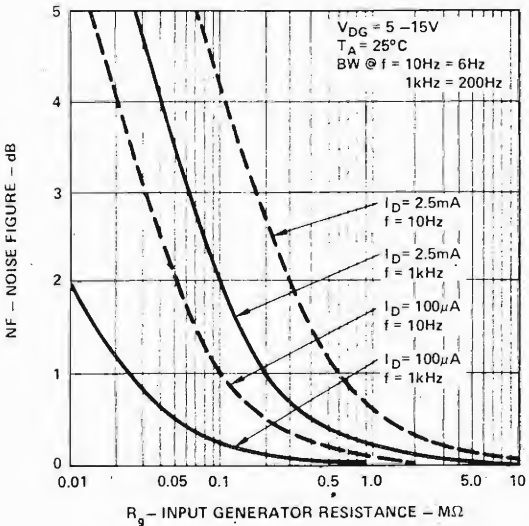



Fig. 5. Comparative Noise Figure

NOISE FIGURE CONSIDERATIONS

For thorough discussion, consult the Teledyne application note "Low Noise FETs — A Challenger to Low Noise Bi-Polars." Since total noise is a function of so many different variables, no direct correlation can be established other than the affect of R_g and f on noise. The main point is that above 500K R_g, the Noise Figure variation is negli-

Operating Value	Units	I_{DSS}	I_D Value 10 mA	–2.5 mA	1.0 mA	0.5 mA	0.2 mA	0.1 mA	Device No.
$V_{GS\ op}$	V	0	—	0	−0.4	−0.65	−0.8	−0.9	A
		0	−0.8	−3.0	−3.6	−3.85	−4.0	−4.1	B
$D_H(\%)$ @ V_{in} = 500 mVpk	%	8.5	—	8.5	11.5	15.0	18.0	21.0	A
		2.5	3.0	6.5	9.0	11.0	12.5	14.0	B
$D_H(\%)$ @ V_{in} = 100 mVpk	%	1.7	—	1.7	2.3	3.0	3.6	4.2	A
		0.5	0.6	1.3	1.8	2.2	2.5	2.8	B

Device No. A – $V_{GS(OFF)} = -1.5$ V, $I_{DSS} = 2.5$ mA; B – $V_{GS(OFF)} = -5.0$ V, $I_{DSS} = 14$ mA

gible. Figure 5 represents a typical plot of the N_F performance on the U1994E, 2N4302 type devices. One can see that in certain areas of application, operating conditions will be designed around operating conditions for minimum noise. Where low noise is the prime criterion for low R_g values, recommend considering the 2N5391-2 type devices.

THE LAST WORD

There are many situations where presently used U1994E, 2N4416 type devices should be replaced with 2N4302, 2N4220 types. In some cases a lower cost unit such as a 2N4304 or 2N3823 unit could be used. Analyze your circuit for its guard banded minimum performance requirements, then pick an appropriate device.

The JFET High Frequency Amplifier/Mixer

The JFET continues to see greater use in small-signal VHF and UHF amplifiers and mixers. Cost is now comparable to the bi-polar and one must consider the advantages of using a FET.

1. **Distortion:** Because the FET follows closely the square law transconductance curve, cross-modulation and inter-modulation distortion is small.
2. **Noise:** With GHz type gain-bandwidth product and majority carrier noise only, low-noise performance exists over the entire frequency range.
3. **Dynamic Range:** The voltage controlled FET provides at least ten times the input-voltage range of the bi-polar.
4. **Input resistance:** When used Common-Source, (CS), high input impedance minimizes interaction with tuned input circuit, and with no power loading.
5. **Detuning:** FETs are insensitive to minor shifts in operating conditions from AGC action — thus minimal detuning is exhibited.

Parameter Considerations

To obtain optimum performance, the designer must consider Gain, Bandwidth, Noise Figure, VSWR, AGC stability, Neutralization, Input and Output Impedances, Distortion and of course, Cost. The Miller Capacitance is a dominant factor in the CS configuration and as such Common Gate, CG, mode is most often used. In FET circuits, standard h.f. circuit techniques are most important. Biasing with chokes is standard for ac isolation.

Most high frequency JFETs such as the 2N3823, 2N4223, 2N4416, 2N5078 and 2N5397 include guaranteed Y-parameter values plus curves of the typical values versus frequency. With these, maximum stable power gain, distortion and neutralization can be determined.

Power Gain

On a stand alone basis, the power gain of a neutralized common-source amplifier is higher up to 600 mmhos than the common-gate. The key is the much higher input admittance on common-gate (i.e. Gig ≈ 4 mmhos at 100-200 MHz, 6 mmhos at 500 MHz, while G is ≈ 0.08 mmhos at 100 MHz, 0.25 mmhos at 200 MHz, 3 mmhos at 500 MHz on the 2N3823, 2N4223, 2N5078; $Y_{fs} = -Y_{fg}$ $G_{os} = G_{og}$).

$$Ap = \frac{|Y_{21}\text{-}Y_{12}|^2}{4\,G_{is}\,G_{os}} \quad \text{(C.S. Neutralized)}$$

$$Ap = \frac{|Y_{21}|^2}{4\,G_{ig}\,G_{og}} \quad \text{(C.G. Un-neutralized)}$$

Unfortunately, the C.S. maximum power gain does not minimize noise. From experience, Ap will be 1-2 dB below max. where NF = minimum. Similarly drain current from 15mA to 3mA will lower Ap ≈ 2dB.

Input Impedance

In the C.G. network, the input impedance in the VHF area is the r_{DS} of the device — usually in the 100-175 ohm range. The C.S. impedance is the capacitive reactance. Most often the FET will be driven from low source impedance, and C.G. minimizes matching problems. Common-gate simplifies low VSWR through the ease in matching input to most signal sources. Networks for critical tuning the C.S. configuration become difficult. The cross-modulation performance is also affected.

Cross-modulation/Intermodulation Distortion

Both types of distortion are proportional to the amplitude of the gate-source voltage, being inversely proportional to the magnitude of the undesired signal at the input. Matching to a high input conductance means low input voltage

High Frequency Ampli/Mixer

Critical Requirement	Preferred High Frequency FET Configuration — Preferred Common-Gate	Configuration Common-Source
Max. Power Gain (Neutralized)		x
Max. Power Gain (Un-neutralized)	x	
High Input Impedance		x
Low Input Impedance	x	
Minimum Distortion	x	
Maximum Stage Stability	x	
Maximum Stage Bandwidth		x
Minimum Noise Figure		x
Best Compromised stage	x	

(i.e. common-gate) and thus low cross-modulation distortion. From the basic FET equations and actual data, greatest cross-modulation rejection occurs when $V_{GS(off)}$ is high and operating, $V_{GS}/V_{GS(off)} = 0.5$. For a typical 2N4416, ID – 3mA.

Stability

In the common-gate configuration, because ReY11 (Gig) is large and ReY12 small, the FET circuit will be stable over the full frequency range. The common-source configuration with low ReY11 is not stable without neutralization until f = 700 MHz for today's FETs.

For the common-source amplifier, the Linvill stability criterion is:

$$C = \frac{|Y_{21}Y_{12}|}{2ReY11Y22 - ReY21Y12} \qquad C > 1 \text{ Unstable} \quad C < 1 \text{ Stable}$$

Bandwidth

In the CS configuration, bandwidth is limited by the effect of input and output impedance matching. Thus maximum bandwidth occurs at the expense of Np and Ap. Virtually no compromise is required in CG where the bandwidth is determined by the circuit Q.

$$Q = \frac{ImY22'}{2\,ReY22'} \qquad BW = \frac{f}{Q}$$

Y22′ = Composite output network

A typical Q = 50 at f = 500MHz. As such a bandwidth of 10MHz can be realized.

Noise

Noise at any frequency is very much a function of input conductance High frequency optimum source conductance varies linearly with frequency, while FET input conductance varies as frequency squared for CS while approximately constant for the CG configuration. Thus common-gate in a non-maximized condition may realize less noise than the CS. The approximate noise figure relationships are given by

$$NF_{CS} = 10 \log \left(1 + \frac{g_{GEN}}{g_{fs}}\right) \text{ (for CS stage)}$$

$$NF_{CG} = 10 \log \left(1 + \frac{1}{1 + \frac{g_{fg}}{g_{GEN}}}\right) \text{ (for CG stage)}$$

CASCODE Common-Source Circuit

A popular technique up to 200MHz utilizing the key features of the common-source stage, is to cascode FETs using the CS input stage with a CG stage acting as its load. This technique produces a 100+ reduction in Miller capacitance, and provides a good broadband un-neutralized CS amplifier. The CS equations still apply where the Y12 is now negligible. The input stage must have the lower I_{DSS} when operating at zero bias to insure adequate drain-source voltage across it.

FET Mixer

The JFET has broad usage in mixer applications, a result of its low input impedance in common-gate mode, wide dynamic range, low distortion, and circuit stability for wide parameter variations.

The low level modulated input signal is mixed with a large local oscillator signal, V_{ol}, and the difference frequency selected by a tuned circuit is further amplified. The resulting modulated lower frequency is extracted and used in the remaining low frequency circuitry.

1. Conversion Transconductance, GC

Power conversion gain is proportional to GC — the ratio of drain current (at output frequency) to input voltage. The oscillator signal level, V_{LO}, directly affects GC.

$$GC = \frac{g_{fso} V_{LO}}{2 \times |V_{GS(OFF)}|} \text{ or substituting } g_{fso} = \frac{2I_{DSS}}{|V_{GS(OFF)}|}$$

$$GC = \frac{I_{DSS} \bullet V_{LO}}{V_{GS(OFF)}^2}$$

2. Noise Figure, NF

To minimize noise figure for a given source resistance, GC should be maximized. Similarly for JFETs, R_S = 800-1000 ohms minimizes noise. Approximate noise figure may be written:

$$NF = 10 \log \left(1 + \frac{K}{g_C R_S} + \frac{R_s}{R_g}\right)$$

K — FET Constant
R_g — Gate Bias Resistance
R_s — Source Resistance

3. Cross-Modulation Distortion

The fourth-order terms produced from true square law characteristic departure result in intermediate frequency cross-modulation distortion. Deviation from perfect curves is a function of bias voltage. Cross-modulation is also inversely proportional to V_{OL} level.

4. Correlation — Optimized Mixer Performance

From the device characteristic equations and experimental results, minimum noise figure and maximum conversion gain occurs at:

$$NF_{min} \doteq GC_{max} \text{ at } \frac{V_{GSop}}{V_{GS(off)}} = 0.8 \quad V_{GSop}\text{—Operating gate bias voltage}$$

$$NF_{min} \text{ at } \frac{V_{GSop}}{V_{GS(off)}} = 1.25 \text{ however, good overall performance at 0.8 level}$$

Lower I_{DSS} units enhance the optimum conversion transconductance, thus the 2N3822 and 2N4222 types become good choices for high frequency mixers.

PRACTICAL VHF-UHF AMPLIFIERS/MIXERS

V_{DG} = 15V
I_D = 4mA
NF Typ 2.1dB
G_{ps} Typ 18dB

C_1, C_2 – 0.8-10pF JFD Model MVM010W
C_3, C_4 – 8-35pF Erie Series 539-002D
C_5, C_6 – 0.005μF Erie (2443-000)
C_7 – 0.001μF Allen-Bradley type FA5C
T_1 – 13 turns, 6/16″ ID, #18 enameled copper wire (air core) tapped 3 turns from top
T_2 – 16 turns, 6/16″ ID #18 enameled copper wire (air core) tapped 4 turns from bottom
R – 500Ω – Pot, 0.5W, Bourns type 3067
RFC – 2.70μH Miller type 9230-30
(Unneutralized)

100 MHz CG Amplifier

V_{DG} = 10V
I_D = 10mA
NF Typ 3.2dB
G_{ps} Typ 10dB

C_1, C_2, C_3 – 0.8 – 12pF Johanson type 2950
C_4, C_5, C_6, C_7 – 1000pF Allen-Bradley type SS5D
$RFC_{1,2}$ – 0.15μH Delevan type 1537-00
L_1 – 1.5" long; #16 copper
L_2 – 1.2" long; #16 copper
L_3 – 2.0" long; #22 copper enamel, loosely coupled to L_2, 0.75" spacing

450 MHz CG Amplifier

L_1 – 1.4" long; #22 enamel, close coupled to L_3
L_2 – 1.6" long; #22 enamel, close coupled to L_3
L_3 – 1.75" long; #16 copper
T_1 – Primary, 13T; #22 enamel, close wound on 1/4" form ≃ 1μH
Secondary, 3T; #22 enamel, close wound over primary
C_1, C_2, C_3, C_4, – 0.8 to 12pF; Johanson type 2950

Common-Source Mixer

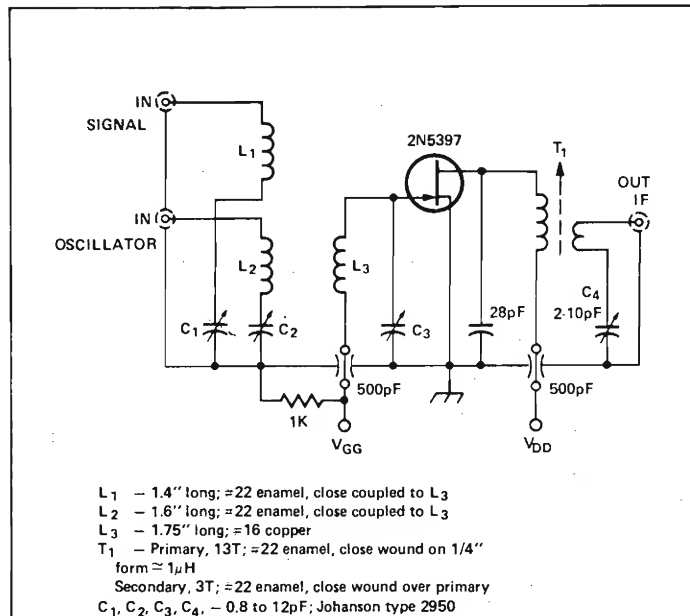
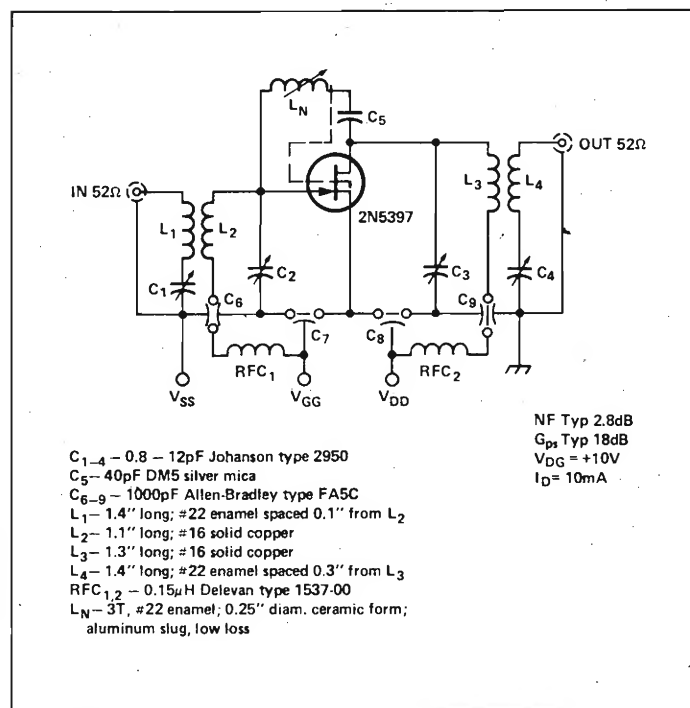
L_1 1-1/2 turns, #20 tinned wire, 1/4 ID, Length = 3/8"
L_2 3-1/2 turns, #18 tinned wire, 3/8" ID, Length = 1/2"
Tapped at 1-1/4 turns from drain

NF Typ 1.5dB
G_{ps} Typ 18dB
V_{DS} = +15V
V_{GS} = 0

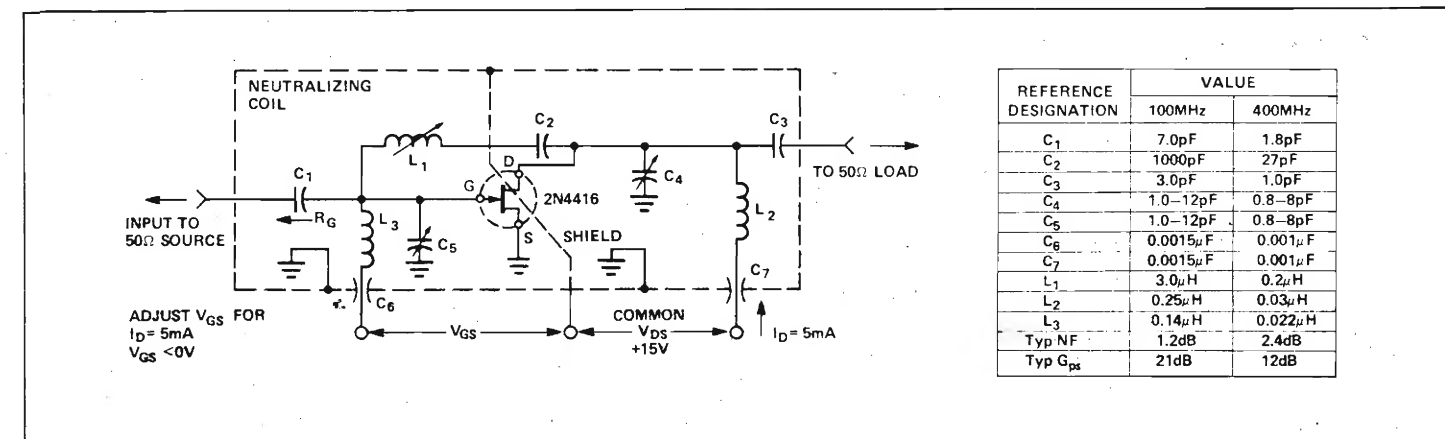
200 MHz Neutralized CS Amplifier

NF Typ 2.8dB
G_{ps} Typ 18dB
V_{DG} = +10V
I_D = 10mA

C_{1-4} – 0.8 – 12pF Johanson type 2950
C_5 – 40pF DM5 silver mica
C_{6-9} – 1000pF Allen-Bradley type FA5C
L_1 – 1.4" long; #22 enamel spaced 0.1" from L_2
L_2 – 1.1" long; #16 solid copper
L_3 – 1.3" long; #16 solid copper
L_4 – 1.4" long; #22 enamel spaced 0.3" from L_3
$RFC_{1,2}$ – 0.15μH Delevan type 1537-00
L_N – 3T, #22 enamel; 0.25" diam. ceramic form; aluminum slug, low loss

60 MHz Cascade Amplifier

450 MHz Common-Gate Amplifier

ADJUST V_{GS} FOR
I_D = 5mA
V_{GS} <0V

REFERENCE DESIGNATION	VALUE	
	100MHz	400MHz
C_1	7.0pF	1.8pF
C_2	1000pF	27pF
C_3	3.0pF	1.0pF
C_4	1.0–12pF	0.8–8pF
C_5	1.0–12pF	0.8–8pF
C_6	0.0015μF	0.001μF
C_7	0.0015μF	0.001μF
L_1	3.0μH	0.2μH
L_2	0.25μH	0.03μH
L_3	0.14μH	0.022μH
Typ NF	1.2dB	2.4dB
Typ G_{ps}	21dB	12dB

100 MHz & 400 MHz Neutralized CS Amplifier

Source-Follower Circuits

The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors.

By considering 10 circuits, which represent virtually every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Fig. 1). Circuits 1a through 1e have no gate feedback; their input impedances, therefore, are equal to R_G. Circuits 1f through 1k employ feedback to their gates to increase the input impedance above R_G.

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Fig. 1:

- Circuits a, d and f can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals, limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, e, h, j, and k employ current sources to improve drain-current (I_D) stability and increase gain.
- Circuits d, e and k employ FETs as current sources. In circuit d, Q_2 must have a lower pinch-off voltage, V_P, and a lower zero gate-voltage drain current, I_{DSS}, than Q_1.
- Circuits e, g, h and k employ a source resistor, R_S, which may be selected to set the quiescent output voltage equal to zero.
- Circuits e and k use matched FETs. R_S is selected to set I_D near the specified low-drift operating current. The input-output offset is zero.

Biasing Without Feedback Is Simple

The no-feedback circuits of Fig. 1 (circuits 1a through 1e) use simple biasing techniques. Circuit 1a is a self-bias configuration; the voltage drop across R_S biases the gate (which draws essentially zero current) through resistor R_G. Since no gate-to-source voltage, V_{GS}, can be developed when $I_D = 0$, the self-bias load line passes through the origin (Fig. 2). For the 2N4339 FET, whose limiting transfer characteristics are used throughout this note, the quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1 kΩ source resistor is used. The quiescent output voltage lies between +0.25 and +0.55 V.

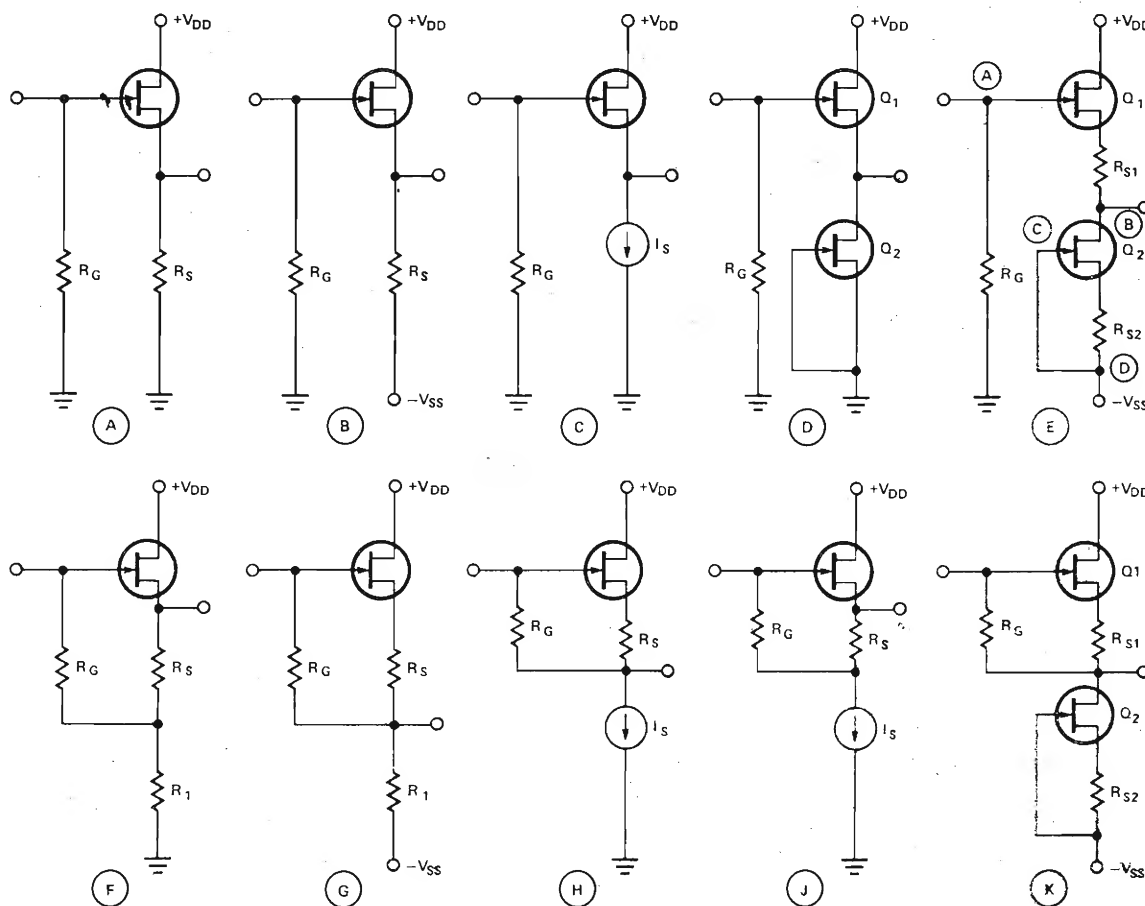



Fig. 1. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

Circuit 1b is another example of source-resistor biasing with a $-V_{SS}$ supply added. The advantage over circuit 1a is that the signal voltage can swing negative to approximately $-V_{SS}$. Two bias lines are shown in Fig. 3, one for $V_{SS} = -15$ V and the other $V_{SS} = -1.6$ V. For the first case, the quiescent output voltage lies between +0.18 and +0.74 V. For the second, it lies between +0.3 and +0.82 V.

The bias load line for circuit 1c is just a horizontal line (I_D = constant). The quiescent output voltage is between +0.15 and 0.7 V for $I_D = 0.3$ mA.

Circuit 1d is similar to 1c except that the $V_{GS} = 0$ output characteristic of FET Q_2 is used as a current source. As seen in Fig. 4, Q_2 does not supply constant current when its V_{DS} gets very small. This technique therefore should be used only to bias FETs whose V_P is significantly higher than the equivalent V_P of the current-source FET diode.

A pair of matched FETs is used in the circuit of Fig. 1e, one as a source follower and the other as a current source. The operating drain current (I_{DQ}) is set by R_{S2}, as indicated by the load line of Fig. 5. The drain current may be anywhere from 0.20 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however, $V_{GS1} = V_{GS2}$ because the FETs are matched.

Since $I_{D1} = I_{D2}$ and $V_{GS1} = V_{GS2}$, choosing $R_{S1} = R_{S2}$ will ensure that the voltage from point A to B equals the voltage from point C to D (Fig. 1e). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating I_D, the source follower will exhibit zero or near-zero temperature drift.

Biasing With Feedback Increases Z_{in}

Each of the feedback-type source followers (Fig. 1f through 1k) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case, R_G is returned to a point in the source circuit that provides almost unity feedback to the lower end of R_G. If R_S is chosen so that R_G is returned to zero dc volts (except in circuit f), then the input/output offset is zero. R_1 is usually much larger than R_S.

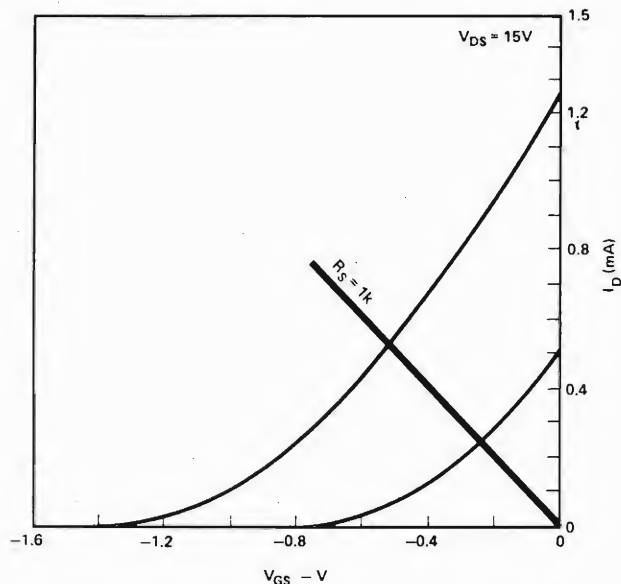



Fig. 2. Self biasing (Fig. 1a) uses the voltage dropped across the source resistor, R_S to bias the gate. The load line passes through the origin and has a slope of $-1/R_S$.

Circuit 1f is useful principally for ac-coupled circuits. R_S is usually much less than R_1 to provide near-unity feedback. The bias load line is set by R_S (Fig. 6). The output load line, however is determined by the sum of R_S+R_1. The feedback voltage V_{FB}, measured at the junction of R_S and R_1, is determined by the intercept of the R_S+R_1 load line with the V_{GS} axis. The quiescent output voltage is $V_{FB}-V_{GS}$.

In the circuit of Fig. 1g, R_S can be trimmed to provide zero offset. As the curves show (Fig. 7), R_S will be between 670 ohms and 2.5 kΩ. R_S is much less than R_1. The source load line intercepts the V_{GS} axis at $V_{SS} = -V_{GG} = -15$ V.

Circuit 1h is almost the same as 1g; the difference is that resistor R_1 is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve

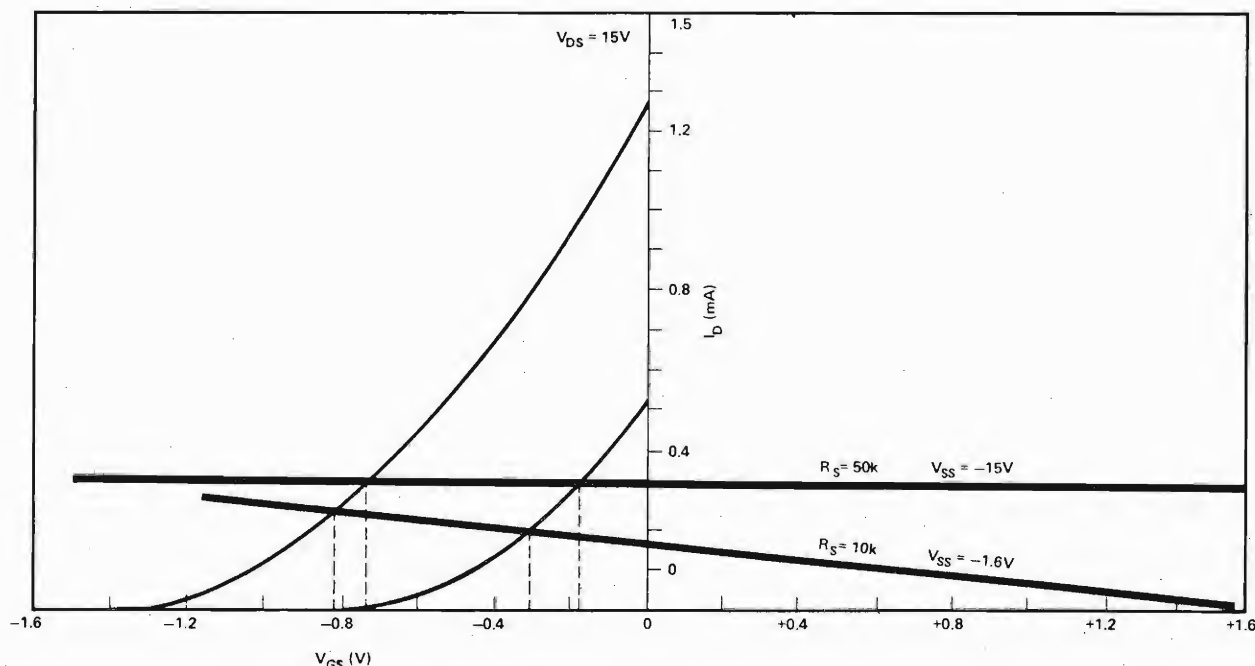



Fig. 3. Adding a V_{SS} supply to the self-bias circuit (Fig. 1b) allows it to handle large negative signals. The load line's intercept with the V_{GS}-axis is at $V_{GS} = -V_{SS}$. Bias lines are shown for $V_{SS} = -15$ V and $V_{SS} = -1.6$ V.

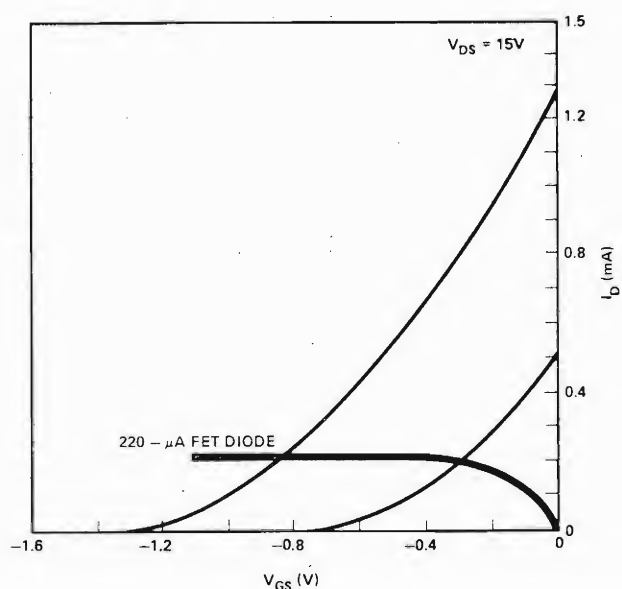



Fig. 4. FET Q_2 doesn't behave like an ideal current source when its V_{DS} gets very small (Fig. 1d). Therefore, Q_1 should have a significantly larger V_P than Q_2 does.

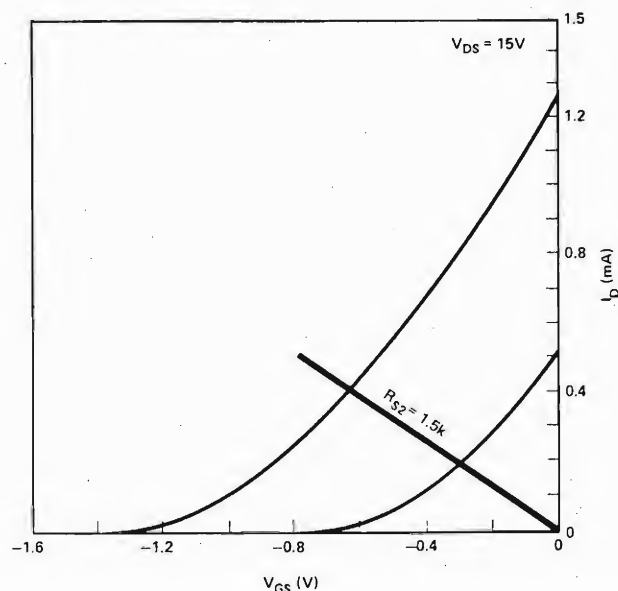



Fig. 5. This load line is set by R_{S2} and Q_2 which acts as a current source (Fig. 1e). If its components are properly matched, the circuit will have zero or near-zero offset.

f circuit 1h differs from that of Fig. 1g (Fig. 7) in that the load line is perfectly flat. In Fig. 7 the load line is almost, ·ut not quite, flat; it has a slope of −1/50 k.

Circuit 1j is similar to 1h except that the output is taken ırom the top of R_S to reduce the output impedance. R_S must be trimmed if the circuit is to work at all properly.

In Fig. 8, the constant-current load line represents a .3 mA current source, and the effect of a 1 kΩ source resistor is shown. The offset voltage is seen to lie between ∩.2 and 0.75 V. The intercept of the R_S load line and the V_{GS} axis sets the voltage at the junction of R_S and the current source (V_{FB}). For $R_S = 1$ kΩ, V_{FB} will be between −0.1 V and +0.45 V. Since V_{FB} appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved.

This can be done by trimming R_S, as shown by dashed lines in Fig. 8. The biasing then becomes the same as for circuit 1h.

Biasing for circuit 1k is identical to that for circuit 1e (Fig. 5) except that feedback is added to raise the input impedance.

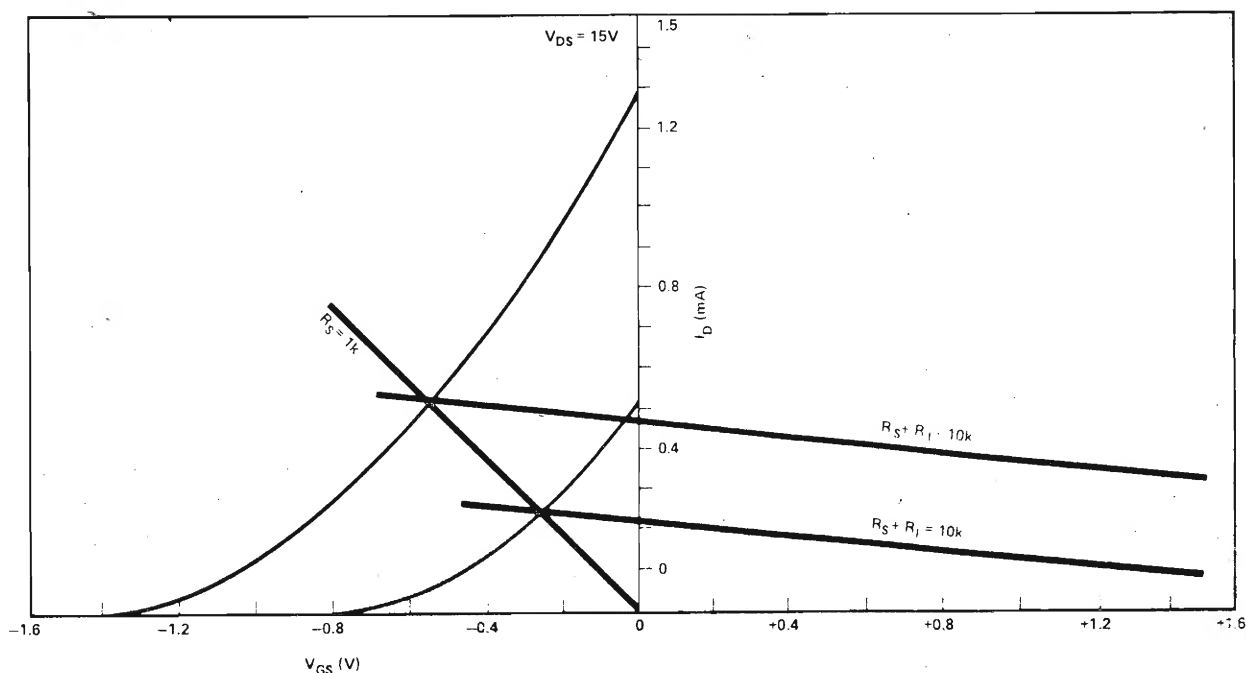



Fig. 6. The bias load line is set by R_S but the output load line is determined by R_S+R_i when gate feedback is employed (Fig. 1f). The feedback V_{fb} is determined by the intercept of the R_S+R_i load line and the V_{GS} axis.

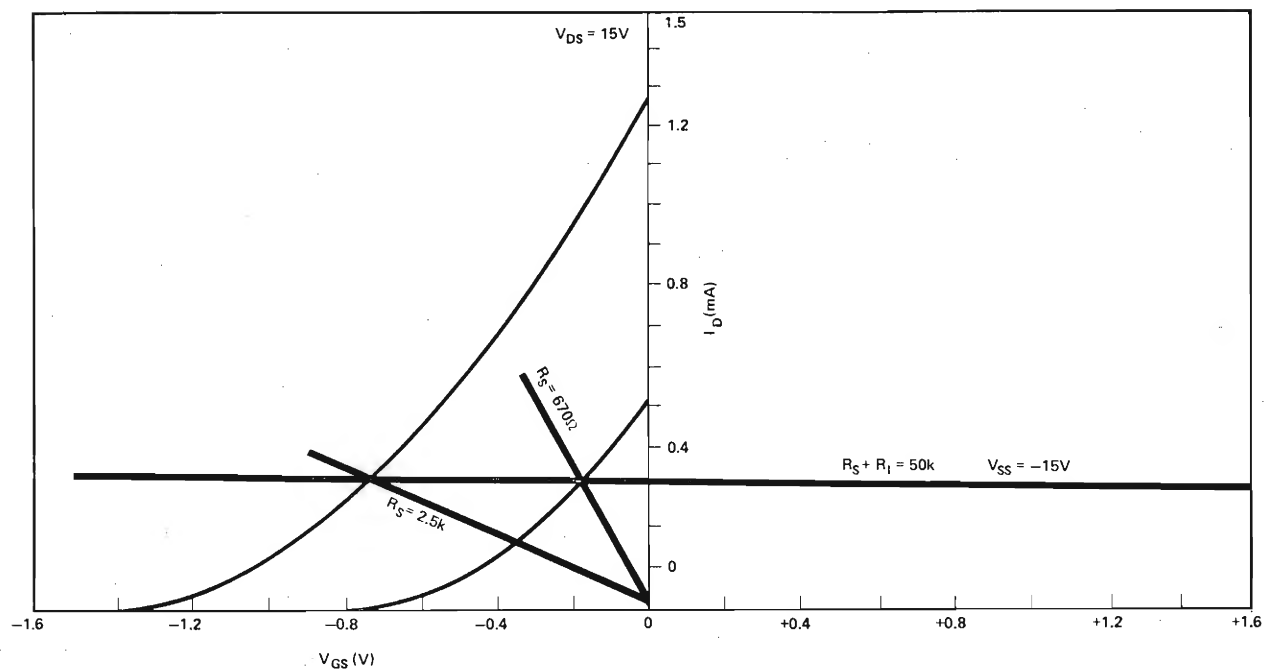



Fig. 7. R_S can be trimmed to provide zero offset at some point between 670 ohms and 2.5 kΩ (Fig. 1g). The source load line intercepts the V_{GS} axis at $V_{SS} = V_{GG} = -15$ V. Note that this load line is not perfectly flat. It has a slope of −1/50k, because the current source is not perfect; it has a finite impedance.

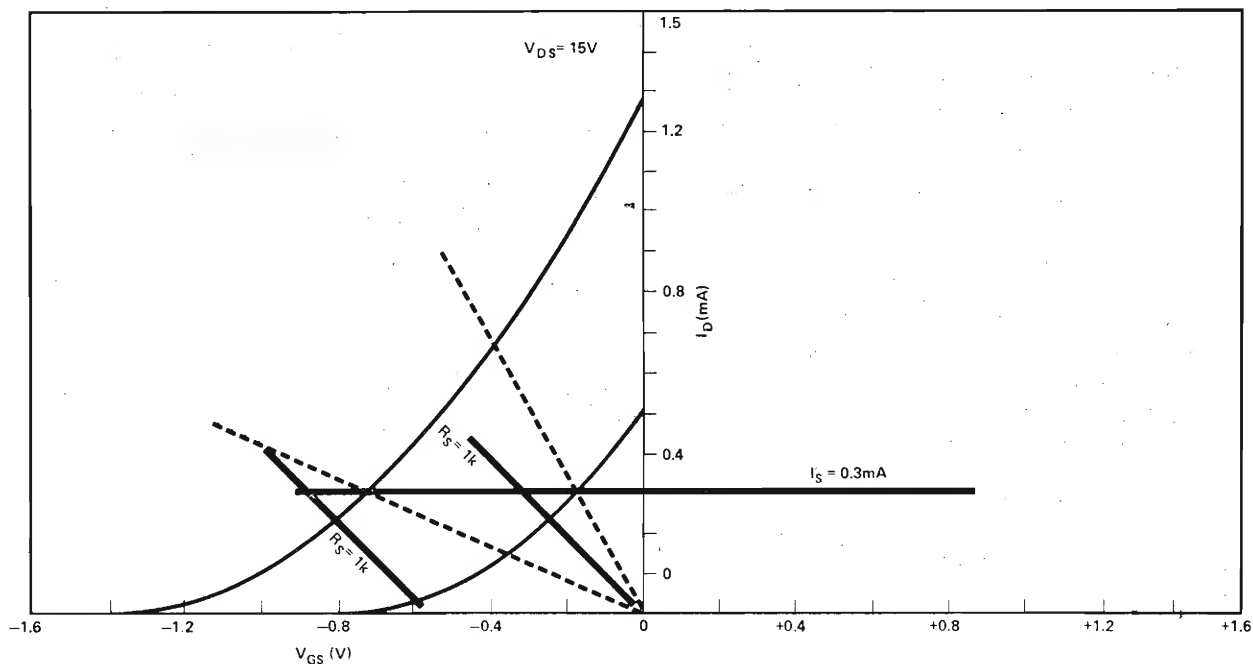



Fig. 8. If R_S isn't trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

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Switches with Junction FETs

I. INTRODUCTION

Ideal switch characteristics are zero ON resistance and zero OFF current or conductance, zero switching time and zero noise.

There are three basic types of switches — or uses for switches: power, logic, and signal. Most logic and many signal switches are commonly known as digital and analog gates, respectively. Other signal switches are generally classed as choppers.

Power applications are primarily concerned with the ON and OFF characteristics of switches, while logic gates are generally more concerned with switching speed. For analog gates and choppers, any or all of these three parameters may be considered important. In addition, isolation from the driving signal — which relates to the output noise level — becomes significant in many applications. Analog gates are commonly used in sample and hold circuits, track and hold circuits, gain changers, remote programming of oscillators, solid-state relays, commutators, A/D and D/A converters, modulators and demodulators, and programmable attenuators.

II. THE FET AS A SWITCH

The junction field effect transistor (FET) is not a perfect switch — but it comes closer than anything else. The OFF current is very low — much less than 100 picoamperes at room temperature, even in quite large devices. The large units also provide lower ON resistance — several types are now available below 5.0 ohms in the 2N5432-4 series. There is no offset voltage in the steady state except what is caused by leakage currents. FETs can be turned ON and OFF in a manner of nanoseconds. The speeds are beginning to rival the fastest injection transistors while still maintaining at least 30 volts of breakdown voltage, higher for specific geometries. Yet the self-isolation feature of the gate input circuit eliminates the bulky, expensive, complex pulse transformer formerly needed with bi-polars. Where speed is not critical, cheap, simple and accurate circuits can be built utilizing FETs.

Steady-State Operation

A junction field effect transistor switch is considered ON when the gate-to-source voltage is zero and the gate-to-drain voltage is low or when the gate is floating. When both voltages are beyond the pinch-off voltage, the device is considered OFF. (Refer to Fig. 1.) When V_{GS} is zero, with a load line as shown, the FET is operating at point A. If the gate is floating. operation is at A'. When V_{GS} is at or beyond $V_{GS(OFF)}$, the device operates cutoff, as at point B. Between these two points, the device is in the active region, acting as either a variable resistor (area I) or as a variable current source (area II).

The slope of either the [$V_{GS} = 0$] or gate floating characteristic at point A or A_1, respectively, defines the ON resistance of the device. When the FET is cut off, the only current flowing in the drain terminal is $I_{D(off)}$, which defines the OFF conductance. $I_{D(OFF)}$ is the sum of I_{DS}, which is essentially zero, and I_{DG}, the drain portion of the gate leakage. (See Fig. 2.) Notice that Fig. 2 shows that $I_{D(OFF)}$ is lower than I_{DGO}. I_{DGO} is the total drain current flowing when I_{SG} exactly cancels I_{DS} so that $I_S = 0$. $I_{D(OFF)}$ is usually measured at a voltage greater than V_F, so that the I_{DS} portion is reduced. Figure 2 is meant only as an illustration of the behavior of the drain and gate terminal currents. None of the curves is exact. (Such curves are almost impossible to measure, because of the requirement that the junction temperature be held constant.)

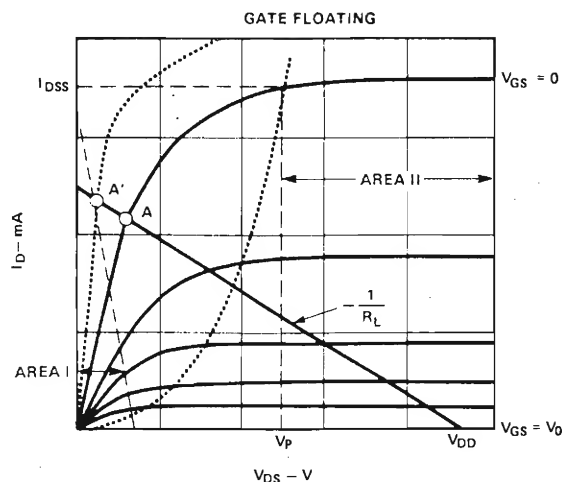



Fig. 1. Family Characteristics.

Fig. 2. Leakage Analysis.

The product of $I_{D(OFF)}$ and r_{DS} (ON resistance at $V_{GS} = 0$) is one figure of merit of a switching FET. It indicates the offset due to devices which are OFF in a multiplex type of application. The total offset, or error, is equal to $I_{D(OFF)}$ r_{DS} times N-1, where N is the total number of channels.

Transient Characteristics

When a FET is switched ON and OFF with a voltage signal, the steady-state points are as discussed above. The transient characteristics deserve some investigation. Con-

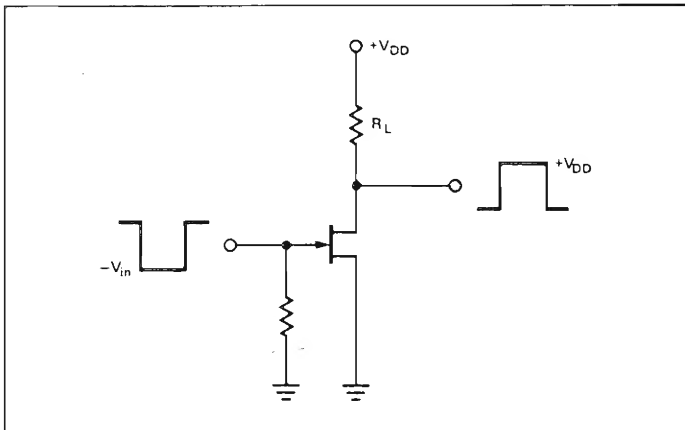



Fig. 3. Simple FET Gate.

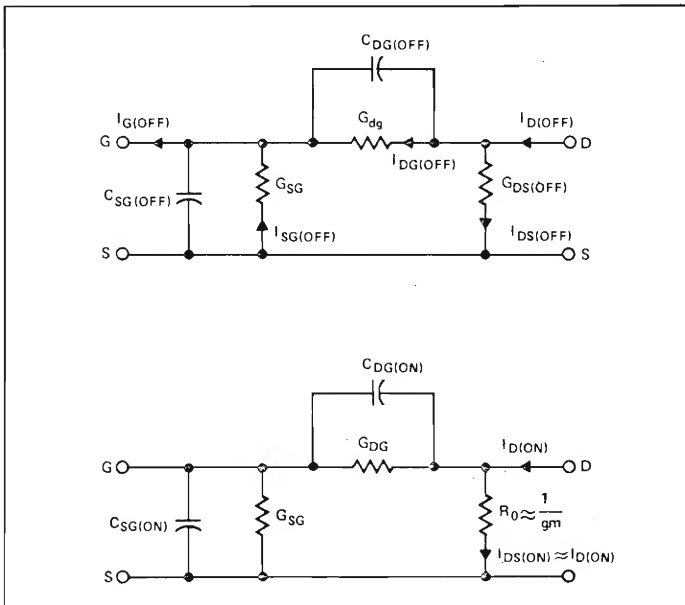



Fig. 4. FET Equivalent Circuit.

sider the circuit of Figure 3 which shows an N channel switch, and examine the lumped parameter FET equivalent circuits of Figure 4. If the device is originally zero-biased (ON), what happens when a turn-off signal is applied?

In our circuit, the source is grounded and the drain is terminated in the load. Obviously, a transient signal will be coupled through C_{DG} to the load, driving the drain voltage lower than it already is. In order to turn the unit OFF, C_{DG} and C_{SG} must be charged to beyond pinch-off. Therefore, the time constant of these capacitances and the series combination of the signal generator impedance R_G, the internal gate resistance r_g, and the parallel equivalent of R_L and r_{DS} will have a major effect on the turn-off time. See Figure 5. The magnitude of the transient seen at the output will be determined by this time constant, the magnitude of the input signal, the rise time of the input signal, and the ratio of the R_L/r_{DS} equivalent to the total series circuit. This transient appears as an excess charge on the stray capacitance always present. The charge must be eliminated and the capacitors all recharged to supply potential before the circuit can be considered OFF. The total transient, including the elimination of the excess charge, appears as a turn-off delay; the subsequent charging of the capacitance to V_{DD} is the circuit fall time. At the end of the transient, the FET is OFF, so the fall time is primarily a function of the time constant of R_L and all the capacitance present at the drain terminal.

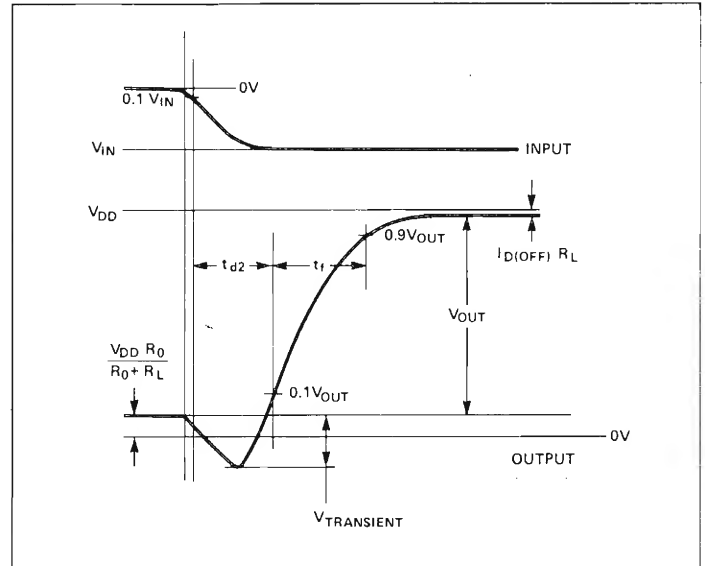



Fig. 5. Turn-off Characteristic.

To turn the device back ON, the procedure must be reversed. The input drive returns to zero and again a signal is coupled to the load through C_{DG}. See Figure 6. This time the output is driven above V_{DD}. The internal capacitances, particularly C_{SG}, must be discharged before the device can turn ON, so there is also a turn-on delay. Once the gate-source capacitance is taken care of, the device tries to pull I_{DSS} and the capacitance is quickly discharged — eventually through r_{DS} of the FET. Since r_{DS} is generally much less than R_L, the rise time of the circuit is much faster than the fall time. The magnitude of the turn-on transient is a function of the time constant of C_{DG} in series with $R_L + R_G + r_g$, the fall time of the input signal, the magnitude of the input signal, and the ratio of R_L to the series combination of R_L, R_G, and r_g.

Driving the gate with a very high impedance to simulate current drive only verifies that the switching times are dependent on signal generator resistance. For example, a device with r_{DS} of about 30 ohms was tested in the circuit discussed above with $R_L = 1\ K\Omega$ and $V_{DD} = 3$ volts. When driven directly from a 50 Ω source with a 10 volt signal, the device exhibited a turn-on delay (t_{d1}) of 12 nanoseconds, a rise time (t_r) of 5 nanoseconds, a turn-off delay (t_{d2}) of 15 nanoseconds, and a fall time (t_f) of 30 nanoseconds. The

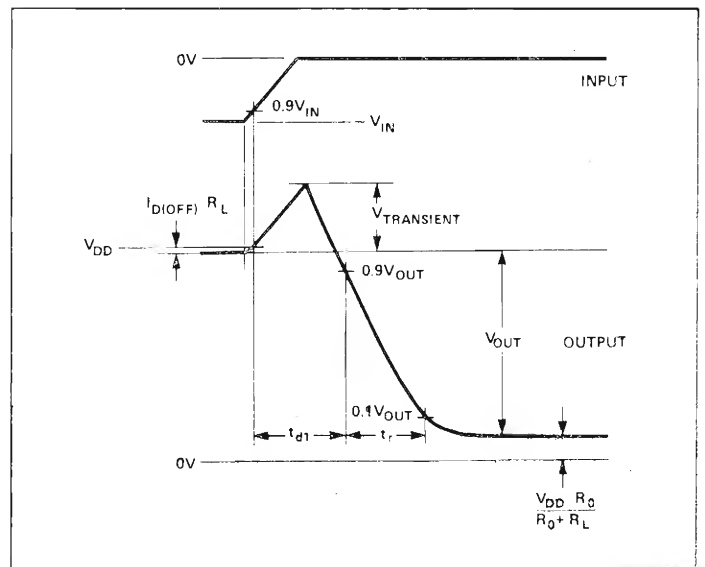
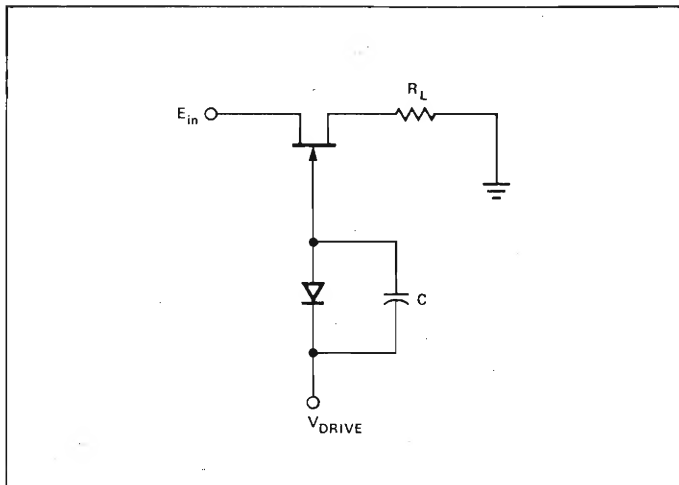
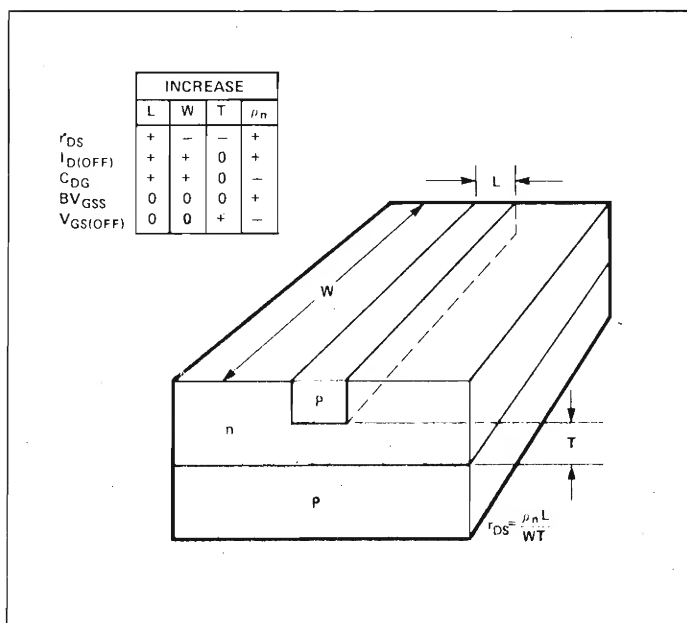



Fig. 6. Turn-on Characteristic.

. 7. FET Gate (Diode isolation).

turn-on trânsient was about 1 volt and the turn-off transient was about 1.4 volts. The same device was operated in the ame circuit except with 1 MΩ in series with the signal generator. Under these conditions, the transient voltages were too low to be seen, t_{d1} was 9.2 microseconds, t_r was 7 microseconds, t_{d2} was 4 microseconds, and t_f was 3 microseconds.

The most useful scheme for driving a junction FET series switch involves the use of a diode for isolating the output rom the drive signal. See Figure 7. When the FET is to be)FF, the diode is biased so that the gate of the FET is clamped to some turn-off voltage. This voltage must be greater than the sum of the pinch-off voltage of the FET and the maximum signal level expected which would tend to turn the device ON. For example, an N channel FET with a 5 volt V_P must have a negative cutoff supply of at least 10 volts to switch a negative 5 volt input. Usually another volt is added to allow for diode drop and power supply variations.

When the device is to be turned on, the diode is reverse biased, letting the gate float and allowing full conduction in the channel. For an N channel to switch a signal up to plus 5 volts, the positive turn-on supply should be greater than 5 volts. Since the reverse biased diode represents a very high impedance, the FET will not turn ON unless some path is provided to the gate for current to discharge the junction capacitance. A capacitor may be placed in parallel with the diode to supply this current. The switching times obtainable in the circuit of Figure 5 in this manner are comparable to the times observed with direct voltage drive.

	INCREASE			
	L	W	T	ρ_n
r_{DS}	+	–	–	+
$I_{D(OFF)}$	+	+	0	+
C_{DG}	+	+	0	–
BV_{GSS}	0	0	0	+
$V_{GS(OFF)}$	0	0	+	–

$$r_{DS} = \frac{\rho_n L}{WT}$$

Fig. 8. FET Parameter Trade-offs.

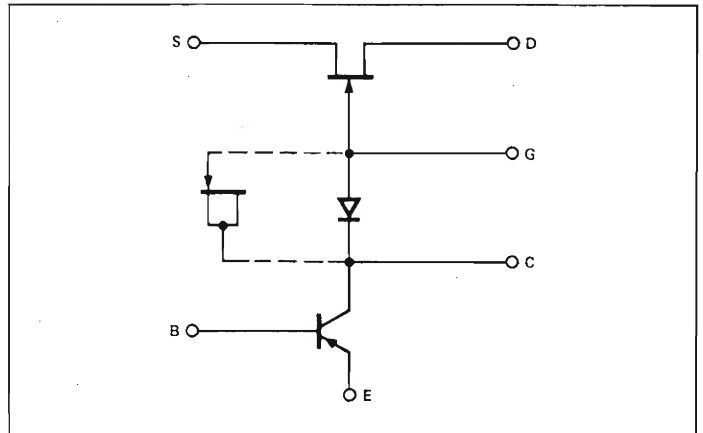



Fig. 9. Basic Analog Gate.

FET Parameter Tradeoffs

Figure 8 shows a very simple drawing of the structure of an FET, and the chart included gives an idea of the compromises possible — within limits — in device design for switching applications. The channel is in the epitaxially-grown N layer; the P substrate serves as the "back" half of the gate. The "top" half of the gate is diffused into the N channel. This diffusion defines the dimensions L, W, and T. The resistivity of the channel, ρn, is basically controlled during epitaxy growth. As can be seen from the chart, a decrease in r_{DS} can be accomplished by an increase in W or T or a decrease in L or ρn. However, increasing W increases leakage and capacitance while increasing T increases pinch-off voltage. Decreasing L is apparently beneficial to leakage and capacitance, but is limited by reliable planar epitaxial techniques. Decreasing ρn decreases breakdown and increases capacitance. Therefore, any change except L — which is a processing limitation problem — involves a compromise with other desirable parameters.

III. ANALOG GATES

The FET Gate

The basic analog gate is shown in Figure 9. This circuit provides the isolation desired between drive signal and switched signal without the use of transformers. Since there is no offset voltage it is possible to transmit signals on the order of microvolts. The basic gate includes an N channel FET switch, the drive diode, and a PNP driving transistor. The resistors and capacitor necessary to complete the circuit are selected to fit the application. The total circuit as shown in Figure 10 has the distinct advantage of requiring no standby current. The only power dissipation in the OFF condition is due to leakage. If the duty cycle is low, such as when a large number of gates are used in a multichannel commutator, overall power dissipation is held to a minimum. An alternate gate using an NPN drive is shown in Figure 11. This circuit minimizes power in the ON condition and is useful when a FET gate is used to replace a relay for an interrupt device which normally remains ON. The circuits described above can also utilize

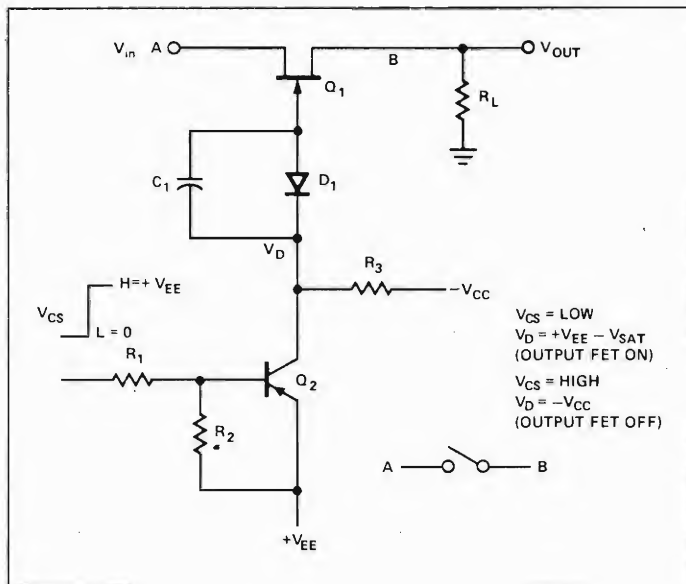



Fig. 10. Complete SPST Analog Gate.

P channel devices, of course. The diode is reversed for such service and the transistors are replaced with opposite polarity types. A single drive transistor can be used to drive more than one FET, if desired, to form switch functions such as SPDT, DPST and DPDT. The connections for these functions are shown in Figures 12, 13 and 14.

Advantages Over Bipolar Gates

The FET gate may be held ON for indefinite periods simply by reverse-biasing the gate input diode. A gate constructed with bipolar transistors which uses a transformer for isolation is limited to an ON time dependent on the transformer circuit. Practically an infinite pulse exists at the transformer second for up to 10 μsec.

Drawbacks

The gate as shown suffers from three effects: (1) turn-on and turn-off are accompanied by voltage spikes in the output load, (2) the ON resistance is temperature sensitive, and (3) the device is not able to respond well to changes in output during the ON time.

The first weakness limits — as a function of sample rate — the minimum signal that can be extracted from the

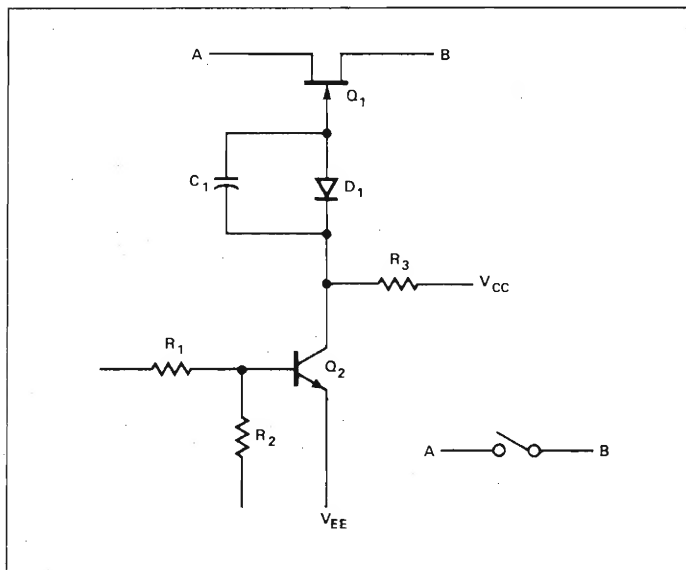



Fig. 11. SPST

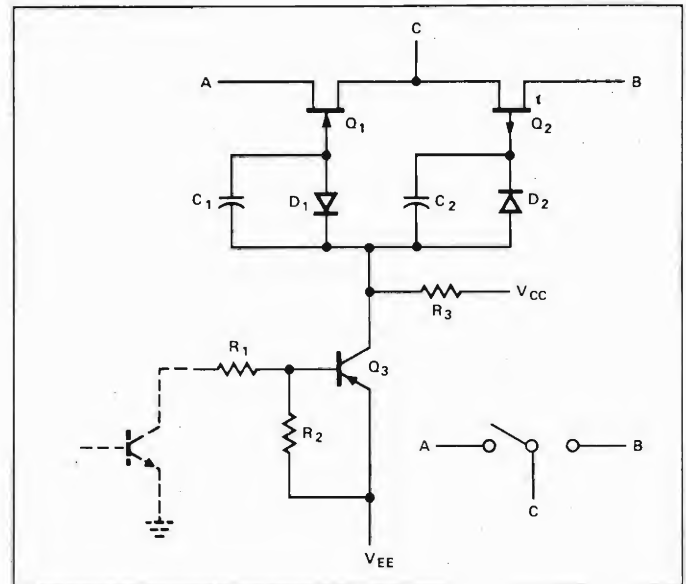



Fig. 12. SPDT

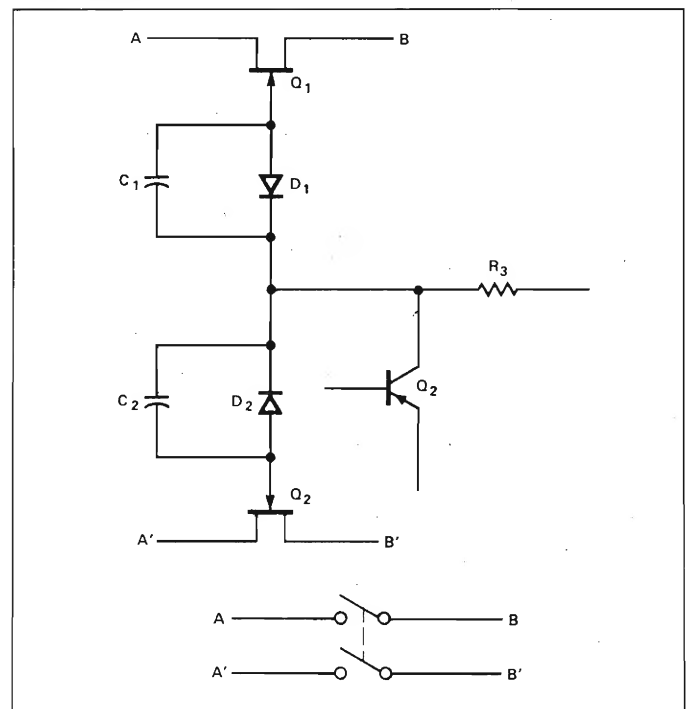



Fig. 13. DPST

switching noise. The second problem is a matter of degree; the absolute resistance change is a function of the geometry. As a percentage of the load resistance, the lower the FET r_{DS}, the lower the error over temperature. The FET temperature and gate bias dependence are:

$$r_{DS\,T} = r_{DS\,amb}(1+0.07\Delta T) \qquad r_{DS\,bias} = \frac{r_{DSo}}{1 + \frac{V_{GS}}{V_{GS(OFF)}}}$$

Referring to Fig. 11, the diode in the gate circuit is necessary for accurate commutation of signals, but, it causes the third problem. With a low leakage diode, the FET takes milliseconds to turn ON, since the gate capacitance must be discharged by the diode's leakage current. So the capacitor is necessary to turn the FET ON in a reasonable time. With the gate ON, C becomes charged to a voltage of V_{EE}-V_{sat}-V_S. Now if the input signal goes positive, the charge on the capacitor holds the gate at the previous level, tending to pinch the device off. The device

will remain pinched off until the capacitor is somehow discharged. The only discharge current available is leakage, however, so this will take some time. The smaller the capacitor is, the shorter the time will be; the minimum value is obtained when only the diode's capacitance is present. A portion of the signal change is coupled to the gate through the Drain-Gate capacitance so that some of the change, at least, gets through.

One Solution

What is needed is a capacitor that has a rather large value at turn-on and a small value during ON time to allow signal changes to be passed. A junction FET itself possesses these traits and is a good low-leakage diode as well. A special FET diode was designed by Teledyne just for this purpose. It is called the FE-30. Substituting the FE-30 for the diode in the analog gate eliminates the need for an external capacitor for turn-on and minimizes the gate clamping action caused by such a capacitor. Under zero bias conditions, the FE-30 has a capacitance value of between 80 and 140 pf; it pinches off to less than 3 pf — comparable to a good general-purpose diode. By carefully selecting the initial capacitance and the pinch-off voltage, a specific amount of charge can be delivered to the FET during the switching time. Teledyne offers the PNP, FET, and special diode as a kit.

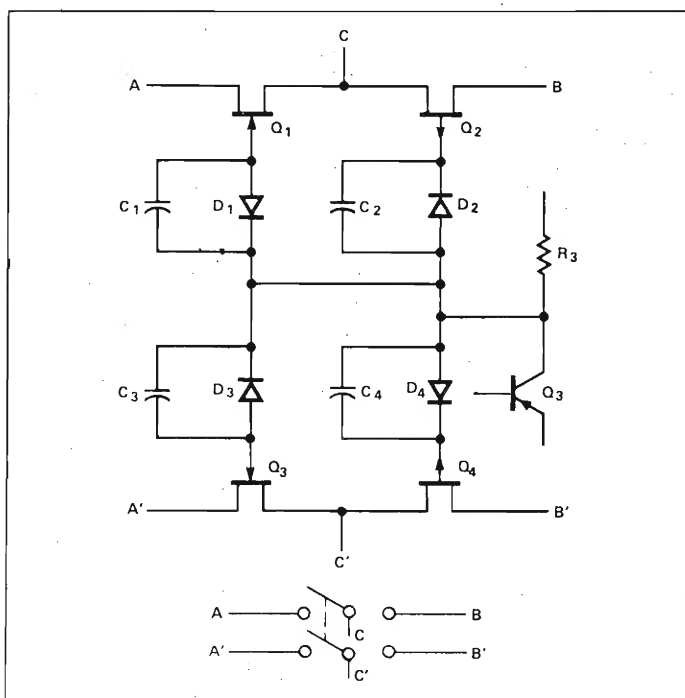



Fig. 14. DPDT

IV. SYSTEM CONNECTIONS FOR IMPROVED PERFORMANCE

If two or more analog gates are connected, as in Figure 15, to a single load in a multiplex type of application, the fact that one of these devices is not wholly cut off while the next one is starting to turn ON increases system speed. The device turning OFF serves to eliminate some of the charge on the stray capacitance, acting as a sort of built-in zero clamp. Charge being supplied to the device coming ON is partly absorbed by the first device also. It is often expedient, therefore, to be sure the turn-off *time* is at least as long as the turn-on *delay*.

If the output of the multiplexer is fed through a unity gain isolation amplifier, the amplifier's output may be fed

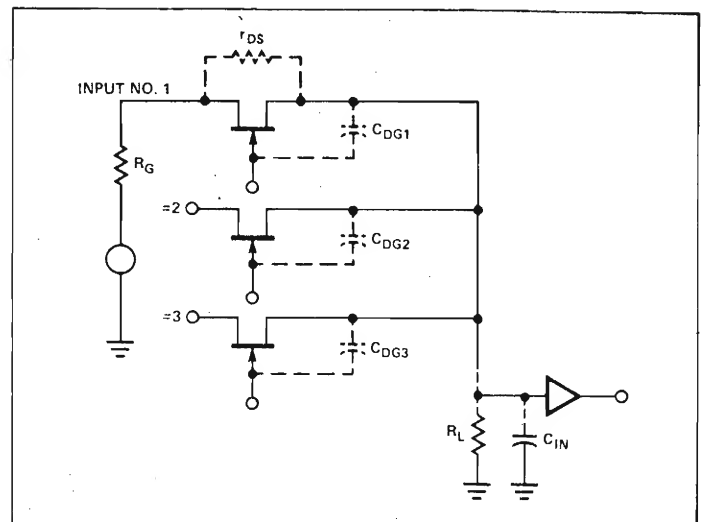



Fig. 15. Multiplexing

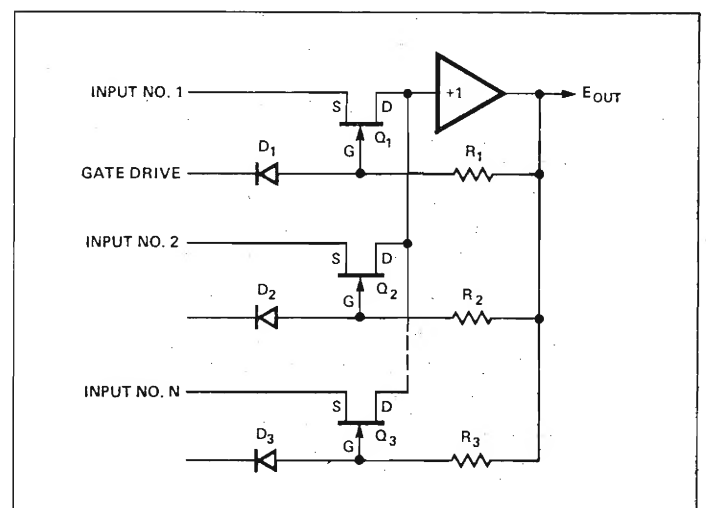



Fig. 16. Multiplexer with Feedback.

to the gate of each FET through separate resistors so that the gate of the one device to be ON is assured of being at source potential. See Figure 16. The drive circuit must allow for the current through the feedback resistors when the gate is to be cut OFF. A current equal to $\frac{2V_{in(max)} + V_{GS(OFF)max}}{R_F}$ must be accounted for to be sure each device is OFF when it is supposed to be OFF.

Figure 17 shows the gates at the summing point of an operational amplifier. This amplifier system performs a part of the multiplexing, provides power gain for the signals (and voltage gain if necessary) and presents an isolating resistance to the transducers in case of a failure in the multiplexer power supply. The FET shown in the feedback path provides compensation for both the ON resistance of the FETs in the gates and their temperature coefficient. Excellent temperature compensation is provided if the devices are from the same family and have approximately the same r_{DS}; tight matching is not required.

Another technique used to improve system performance utilizes the DPST circuit of Figure 13 to operate differentially. See Figure 18 for a circuit diagram of this setup. The desired signal is the difference voltage between the two inputs. This circuit is usful for extracting information from sources that are floating or which have a high common-mode signal. The amplifier must be capable of handling at least one half of the expected common-mode voltage.

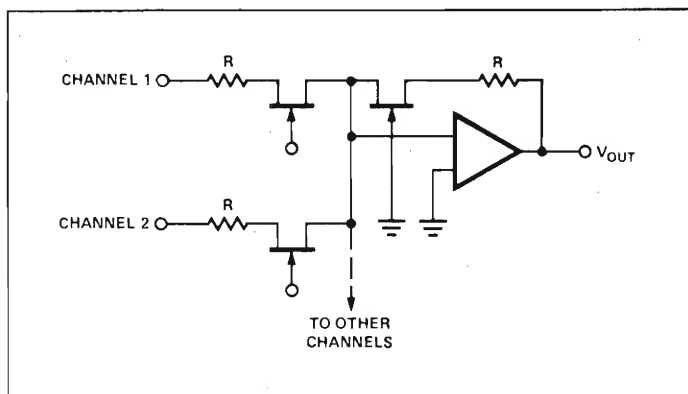



Fig. 17. Multiplexer with Power Gain.

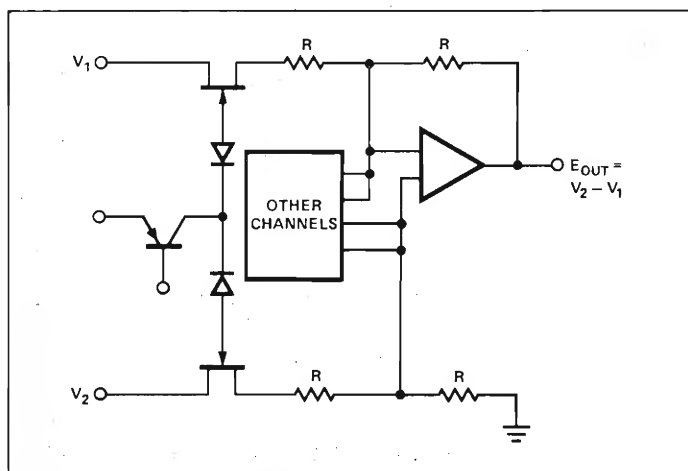



Fig. 18. Differential DPST

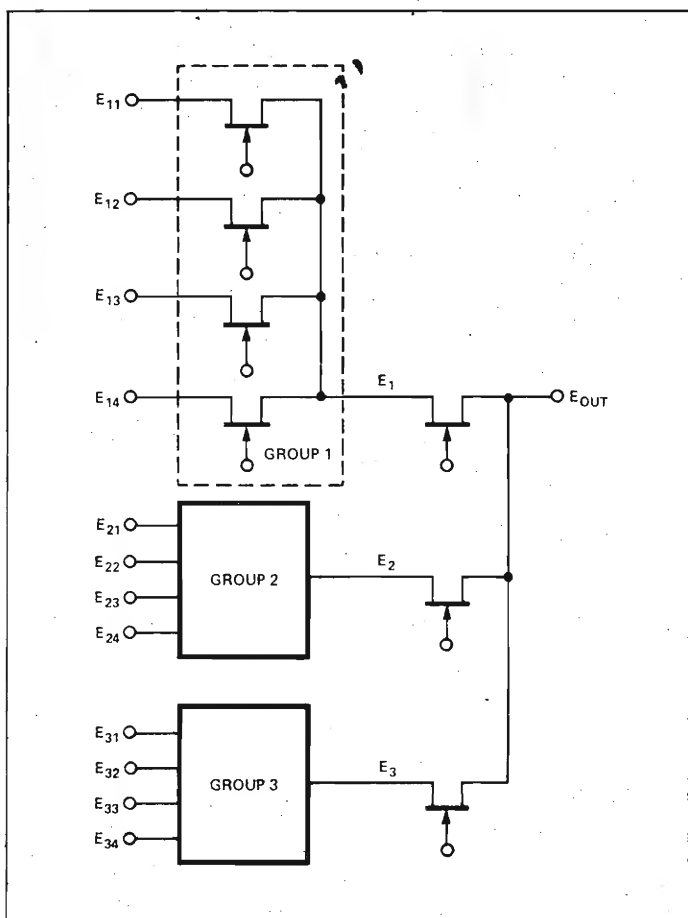



Fig. 19. Submultiplexing (Treeing).

One of the problems with any gating arrangement is the capacitive load that can be handled. Since each added gate adds to the capacitive load, the number of gates that can be fed to a common output is limited by switching speed degradation. One way around this problem is the use of submultiplexing or treeing. The total number of inputs to be multiplexed is divided into manageable groups. See Figure 19. Each group has its own output and buffer circuit, if necessary, and the group outputs are then multiplexed into the final output circuit. More than two levels may be used if a very large number of channels is to be included. The total number of levels is limited by the losses and delays allowed by the system.

AC Signal Range

The ac signal range, for negative peaks, is limited by $-V_{CC}$ being more negative that the most negative input signal, $-V_{in}$, by an amount greater than the FET pinch-off voltage. Consider the case when the coupling diode is reverse biased, which means the output FET is on and an ac signal is on the input. At time t_1 the gate of the FET cannot be any more positive than a diode drop above the channel. This means that the gate voltage is essentially equal to $-V_{IN}$. At time t_2, the input signal is at $+V_{IN}$. If the FET is to remain on, one of the following conditions must occur.

1) $2\,V_{IN} < |V_{GS(OFF)}|$

2) The gate voltage is raised to within $V_{GS(OFF)}$ of $+V_{IN}$.

Since the coupling diode is reverse biased, it can supply only leakage current, and hence will not contribute to the ac swing. Most of the current required to bring the gate positive is supplied by way of c_{sg} and c_{dg} acting as a capacitive divider circuit to the gate from the channel. It is evident that both the stray capacitance from gate to ground, and the off capacitance of the coupling diode play extremely important parts in the ac swing capability because they tend to clamp the gate at the negative potential at time t_1. Extreme care should be taken, at this point, to minimize stray capacitance and to use the proper coupling diode. Our hybrid microcircuit analog gates have both these features.

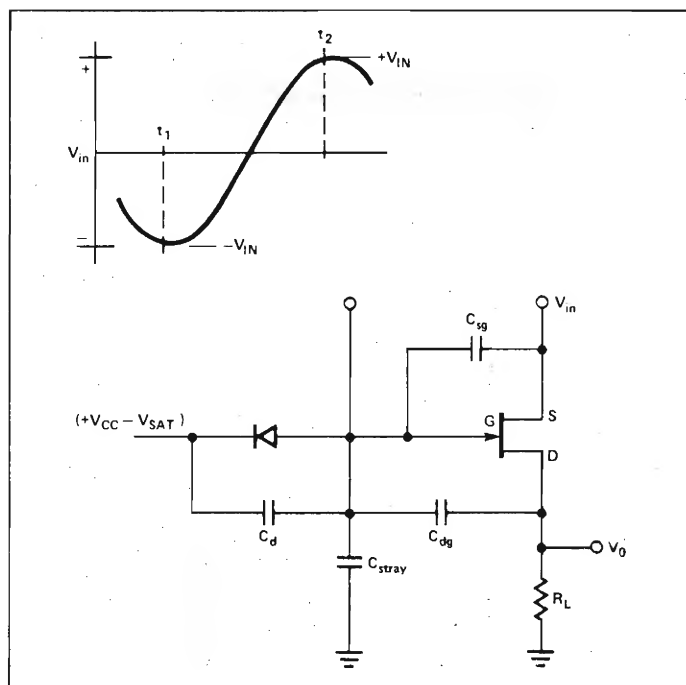



Fig. 20. AC Signal Input.

Referral Resistors

To improve the ac swing, a resistor can be added from the source to the gate of the output FET. This will enable the gate of the FET to track the input signal, so pinch-off will not occur. One drawback is that current can be drawn from the v_{in} signal source when the FET is in the off condition. This is not important, however, if the source impedance is small. The referral resistor should be as large as possible to keep the voltage drop across the 10K resistor small, and also to minimize the current drawn from the signal source.

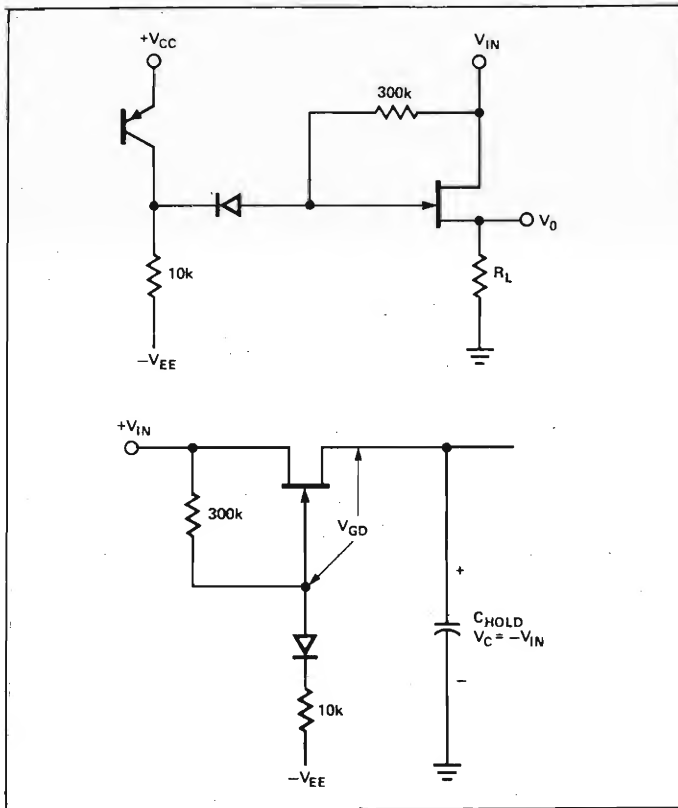



Fig. 21. Referral Resistor.

The worst possible condition for using referrals is when the gate is used in a sample and hold application and is off with the $-V_{IN}$ stored on the hold capacitor. If $+V_{IN}$ is on the input, maximum current will flow through the 10K to $-V_{EE}$, creating a voltage division between the referral and the 10K (neglecting the diode drop). This raises the gate voltage above $-V_{EE}$. Since the output is still negative, the gate must be held more negative by an amount equal to $V_{GS(OFF)}$. This condition is the most difficult to keep pinched-off. With Teledyne Semiconductor's analog gates, use of 300K referral resistor is recommended for most applications. In some cases the analog gate may be used in the shunt mode as in Figure 32. When used in this mode, referral resistors are not required because the on condition of the output FET corresponds to a low impedance path to ground. Hence, no signal swing is required.

Other Gate Arrangements

Figures 22 and 23 show two circuits which use pairs of FETs to solve some of these switching problems. Q_2 from gate to source of Q_1 in Figure 22 replaces the resistor mentioned above. The current in the load during the OFF time is eliminated by this connection, but three new problems arise. More parts are needed: an extra diode and a resistor as well as the extra FET for each gate. An

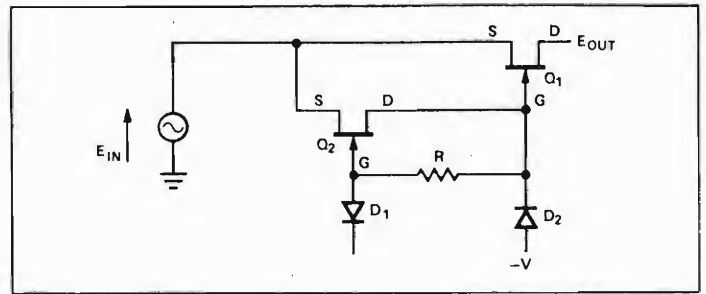



Fig. 22.

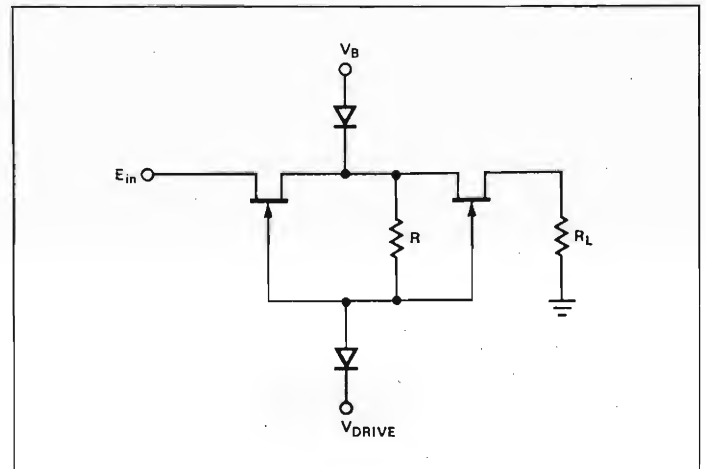



Fig. 23.

extra voltage supply is also required, which must be greater than the sum of the most negative signal to be switched and the maximum pinch-off of Q_1. The input cutoff signal must be greater still by the amount of the maximum pinch-off of Q_2.

The circuit of Figure 23 relieves the cutoff restriction mentioned. The other two problems are still present and another is added: the ON resistance is twice that of one device. This may not be serious.

V. OTHER FET SWITCHING CIRCUITS

Power Switch or Relay Driver

Figure 24 shows an FET with voltage drive used to turn a relay ON and OFF. Three parameters are of major importance: minimum I_{DSS}, maximum $V_{GS(OFF)}$, and BV_{DGO}. The device must be able to handle all the current required by the relay's coil and turn off with the signal to be applied. The inductive kick generated when the relay is turned OFF must be limited to a value below breakdown. This circuit shows the familiar diode/resistor clamp scheme; other methods are also applicable.

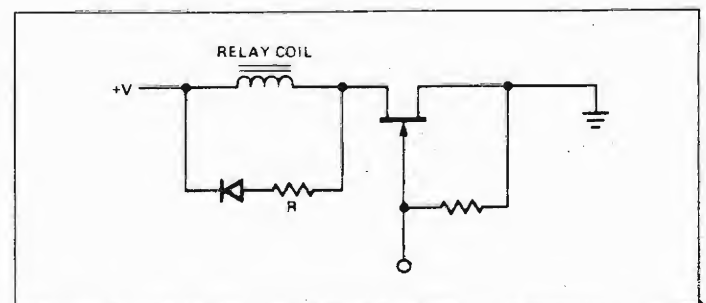



Fig. 24. Relay Driver.

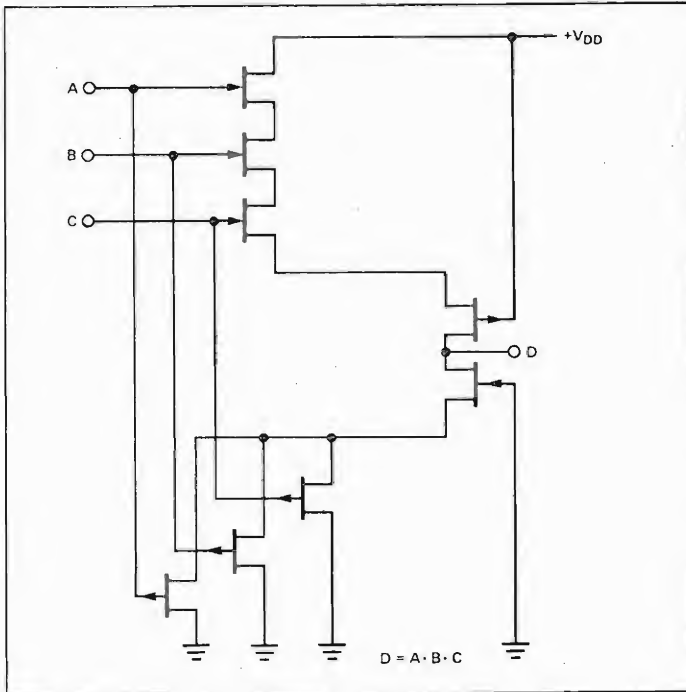



Fig. 25. Three-input AND Gate (positive logic).

Fig. 27. Flip Flop.

Logic Circuits

Figures 25 through 29 show logic circuits using complementary FETs. Figure 25 shows a positive logic three-input AND gate (negative OR), while Figure 26 shows the positive logic OR function (negative AND). These gates draw virtually no power except during switching times since at least one of the series elements is OFF during any state. The input current is only the combined gate leakage of the P and N channel input pair. Therefore, fanout is limited primarily by speed considerations. The critical parameters for the devices in the circuits are $V_{GS(OFF)}$ and r_{DS}. $V_{GS(OFF)}$ must be low enough for the device to turn off when desired, but high enough to provide some noise immunity. The gain must be high enough to provide enough charging current for any capacitance load.

Figure 27 shows a latch circuit (flip-flop). This circuit will remain in the high or low state, as set, until a disturbance is received. Notice that there is only one output — there is no complement. Setting the latch requires a TRUE input to the SET line; resetting requires a FALSE signal on the RESET line.

The circuit of Figure 28 is an inverter and is necessary to provide any required complements, since none exist in the system otherwise. More complex functions than those shown may be formed by combinations of the above circuits. An example is seen in Figure 29, which shows a half-adder or exclusive OR circuit.

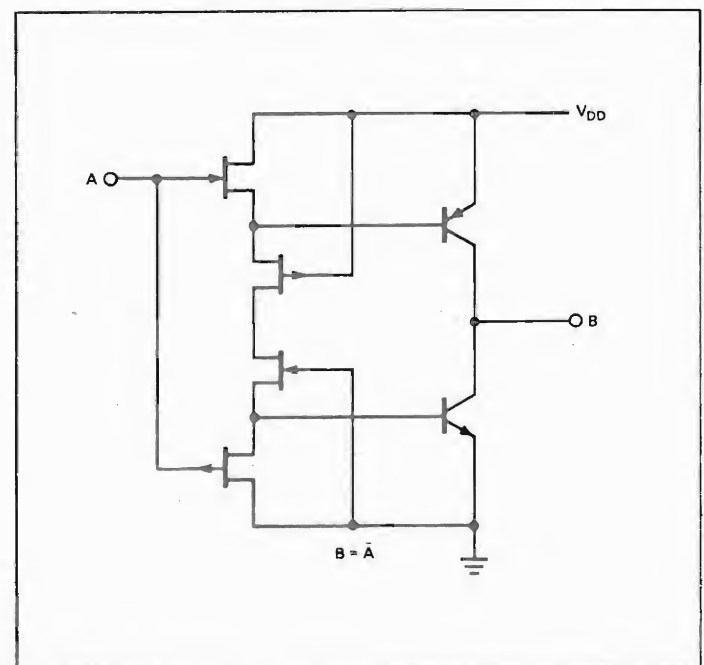



Fig. 26. Three-input OR Gate (positive logic).

Fig. 28. Inverter.

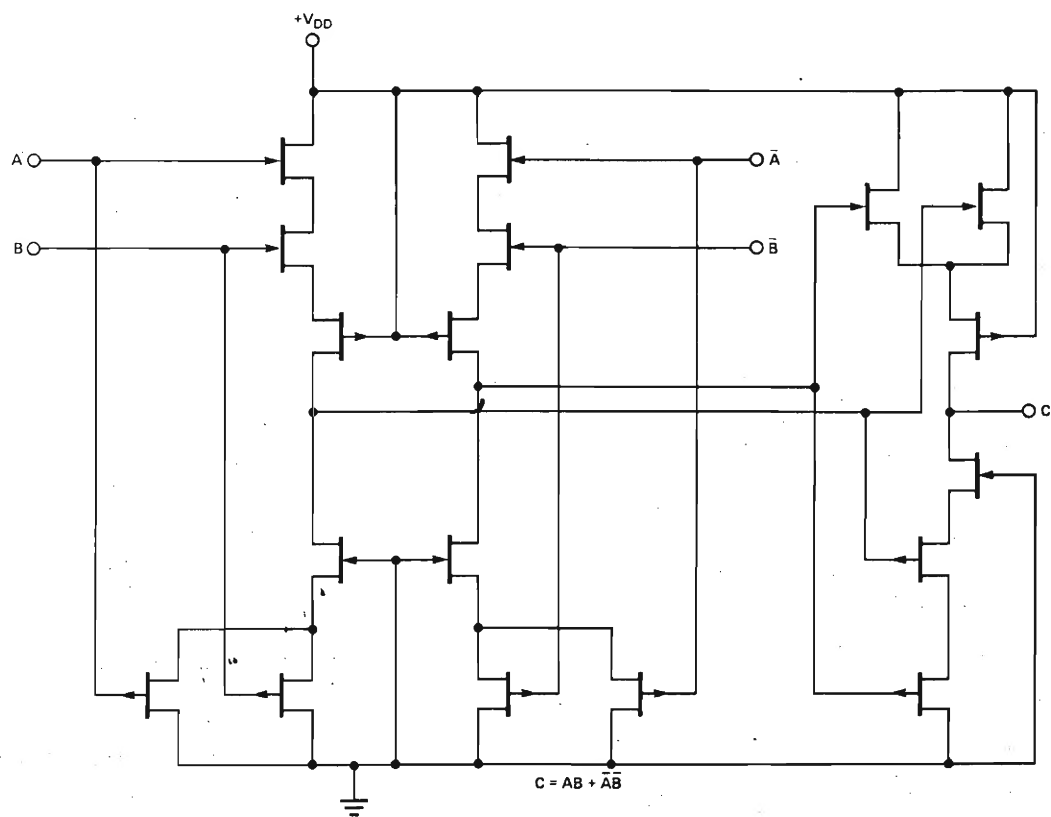
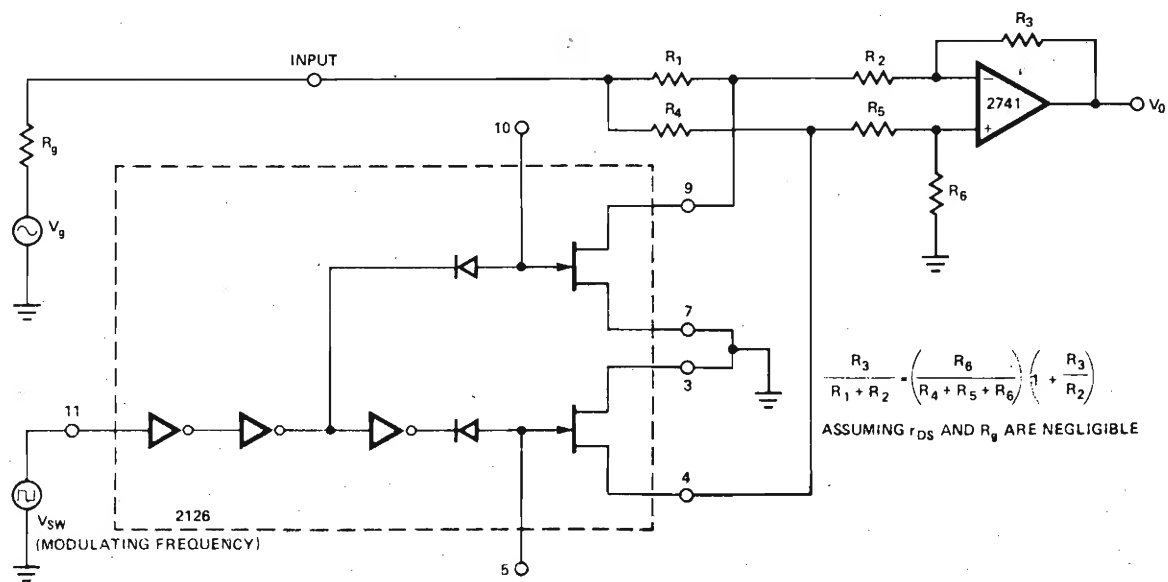
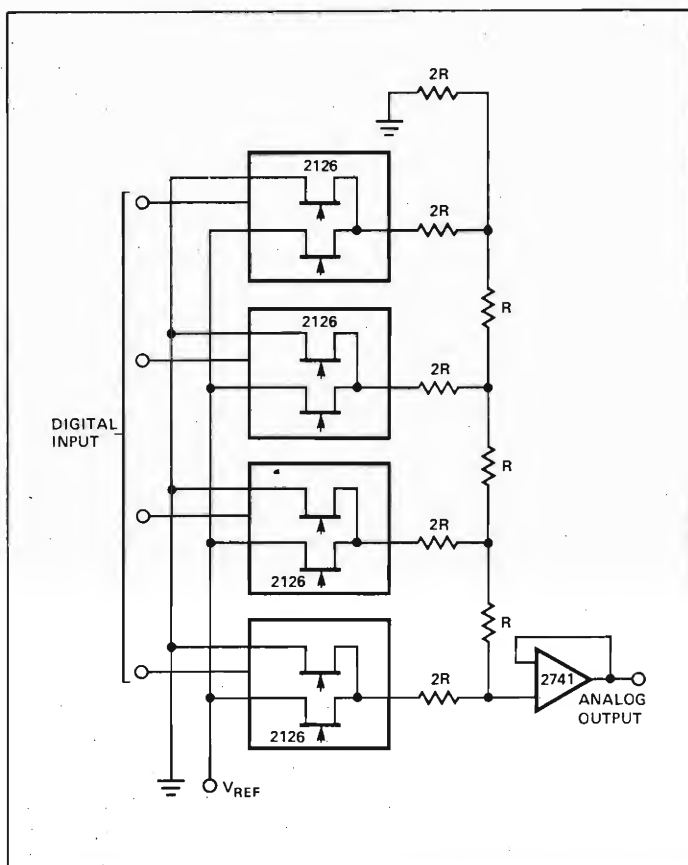



Fig. 31. D/A Converter, Ladder Network.

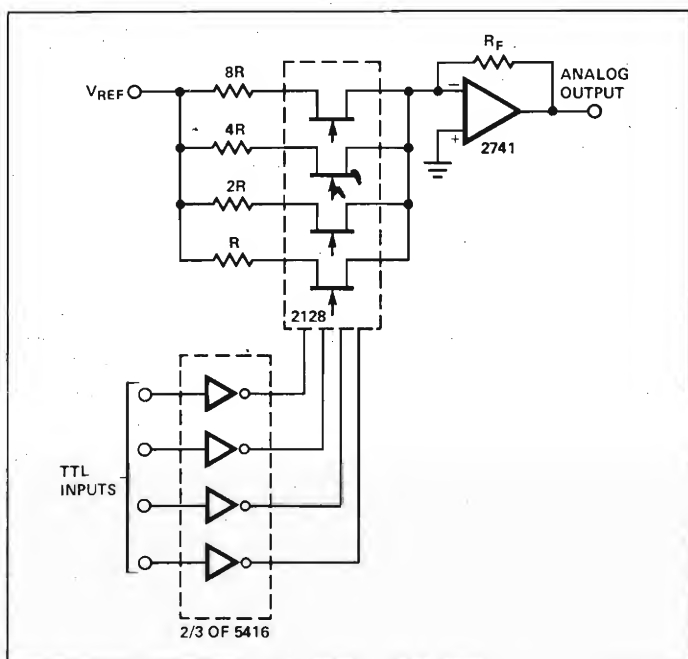



Fig. 32. D/A Converter, Binary Weighted Network.

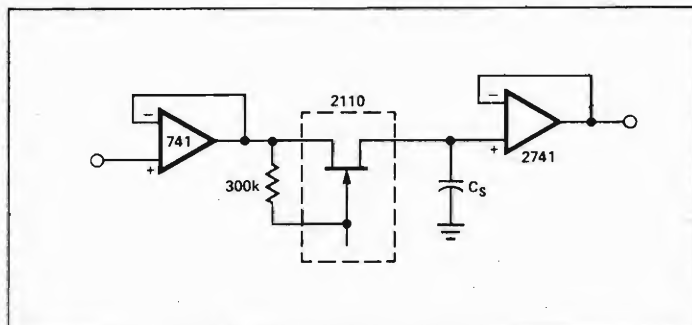



Fig. 33. Sample and Hold Circuit.

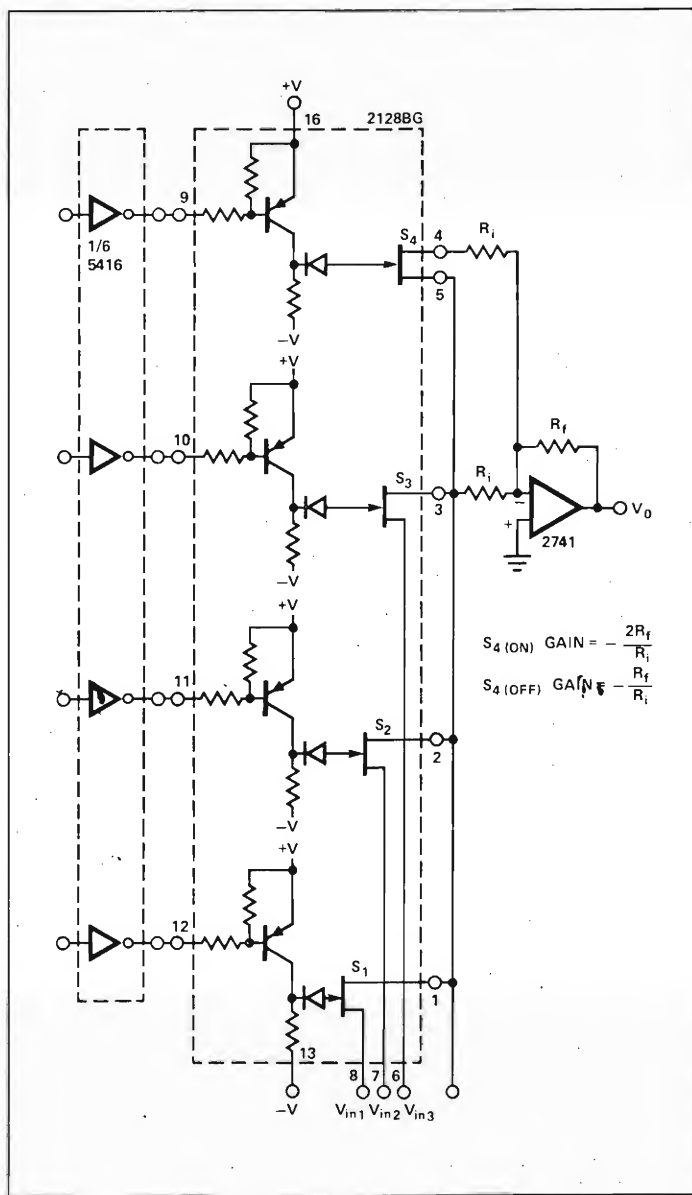



Fig. 34. Three-input Multiplexer With Gain Change.

FET Constant Current Source Limiters

One of the key parameters of a junction field-effect transistor is I_{DSS}, or I_D — the measurement of the drain current with either the gate-source shorted or biased at some desired level. FETs operating at a drain-gate voltage above the device $V_{GS(OFF)}$, on devices designed with low output admittance, make natural current sources. It is also a simple design for layout and operation, being hooked up like a resistor.

USEFUL CHARACTERISTICS AND PARAMETERS

Characteristics of a good current source are: minimum components, high output impedance (log Yos where $r_D = 1/Yos$), operable at low supply voltages, low fixed or adjustable temperature coefficient, and adequate maximum voltage operating range — Fig. 1.

The JFET will meet all these requirements when the proper operating range to give zero temperature coefficient and/or substantial feedback is used to minimize the temperature drift. It is advisable to maintain the current source output impedance (1/Yos) ≥ 50 the maximum load. This will cause a minimal 2-3% change in operating current if the load is doubled.

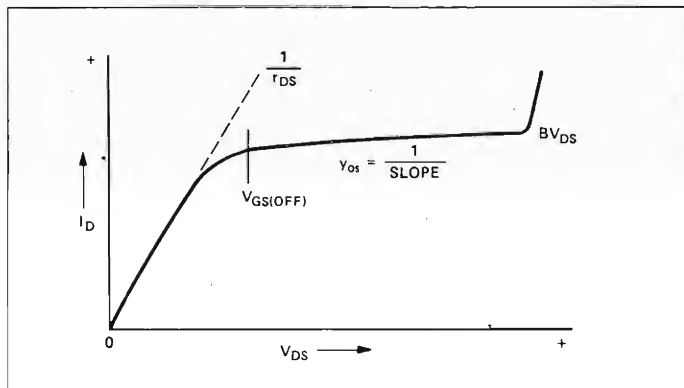



Fig. 1. Current Source Characteristic N-Channel

ZERO TEMPERATURE COEFFICIENT

Much has been said about this characteristic. Basically, there is a drain current, I_{DOTC}, for each device where the change in channel resistance and barrier potential as a function of temperature cancel each other — Fig. 2.

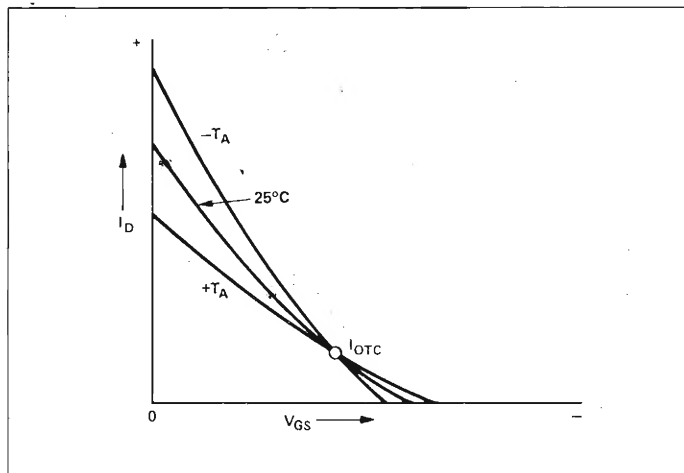



Fig. 2. Transfer Characteristic N-Channel

The current for zero change can be approximated theoretically as $I_{DOTC} = I_{DSS}\left(\frac{.64}{V_{GS(OFF)}}\right)^2$ (Eq. 1) or in terms of V_{GS}

$$V_{GS\,OTC} = |V_{GS(OFF)}| - .64V \quad \text{(Eq. 2)}$$

As one moves away from this current, the gate-source differential drift becomes

$$V_{GS\,D}\ (\mathrm{mV/^\circ C}) = 2.2\left(1 - \sqrt{\frac{I_D}{I_{D\,OTC}}}\right) \quad \text{(Eq. 3)}$$

Through feedback, as is the case for other circuit variations, this factor can be greatly reduced.

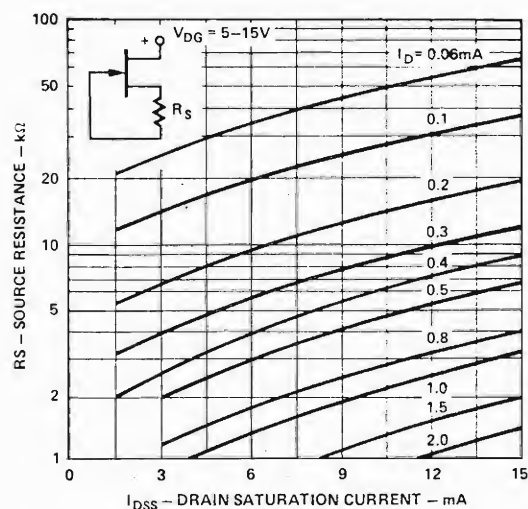



Fig. 3. 2N4220-4, 2N3821-4, 2N4302-4 Current Source Curves

JFET CURRENT SOURCE CONFIGURATIONS

There are methods of varying complexity to maximize different requirements of a current source. One can maximize the output impedance, temperature drifts, and voltage rating. Let's consider the simplest configuration first.

1. The simplest constant current source uses a FET by shorting the gate and source. All the characteristics reflect that of the device, including temperature drift. As such, Equations 1, 2, & 3 apply to this application. One difficulty is that a ±10% I_{DSS} FET is expensive unless you order from the TCR5275-TCR5315 series. Fig. 7.

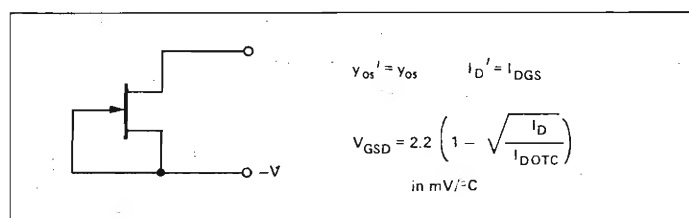



Fig. 4.

2. For other than the TCR Series, a method using a low cost resistor provides for practical operation. Degeneration enhances the device output impedance and reduces temperature drift effects. It is easy to compensate for the I_{DSS} variations of 2N devices by a variable R_S for exact settings, or by choosing one of 3 resistors to match the I_D range. Plotted in Fig. 8 is the 2N4220-4, 2N3821-4 and 2N4302-4 series.

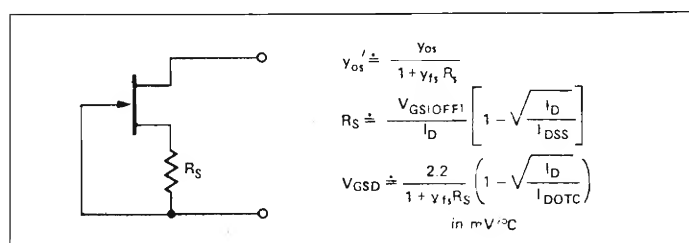



Fig. 5.

3. Where the output impedance or BV of Fig. 5 is not satisfactory (rarely the case), one of the configurations of Fig. 6 can be used. The drain current will be that of Q_2, BV of Q_1. It is important in Fig. 6a that the $-V_{GS}$ of Q_1 be greater that the $V_{GS(OFF)}$ of Q_2. Fig. 6b is a method to circumvent that problem.

(a) (b)

$$Y_{os} \doteq \frac{Y_{os}^2}{Y_{fs}\,(1 + R_S Y_{fs})} \qquad R_S \doteq \frac{V_{GS(OFF)}}{I_D}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$V_{GSD} \doteq \frac{2.2}{1 + Y_{fs} R_S}\left(1 - \sqrt{\frac{I_D}{I_{DOTC}}}\right)$$

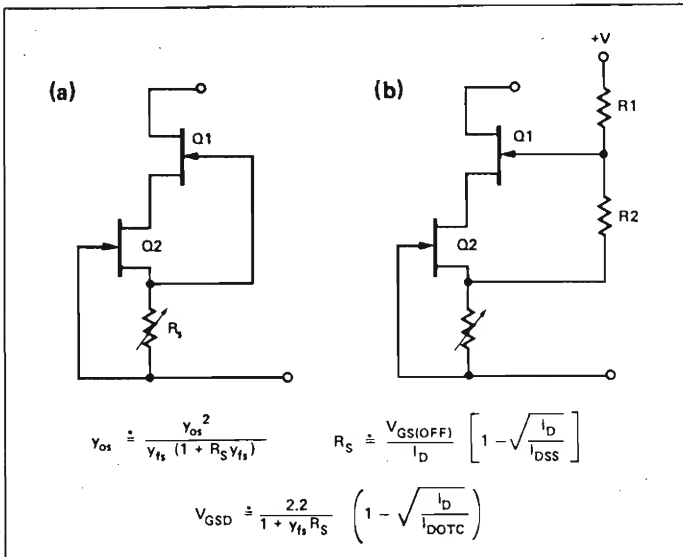



Fig. 6

4. The TCR5275-TCR5215 is a series of two-terminal TO-18 can current regulators from 40 μA - 5.72 mA in 10% increments. Available as chips, the one lead bond makes them ideal for hybrid use. The data sheet indicates up to 25MΩ guaranteed output impedance. As is the case for any configuration, devices may be paralleled to minimize temperature coefficients. Zero TC crossover occurs at 400-500 μA.

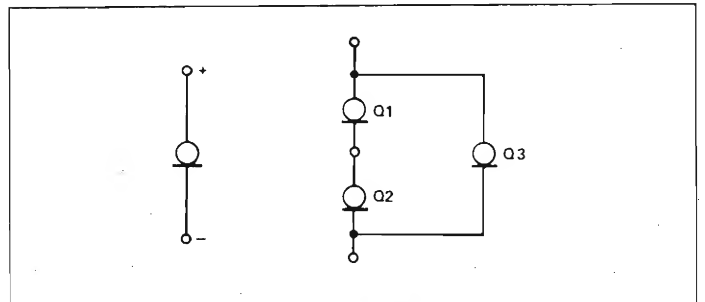
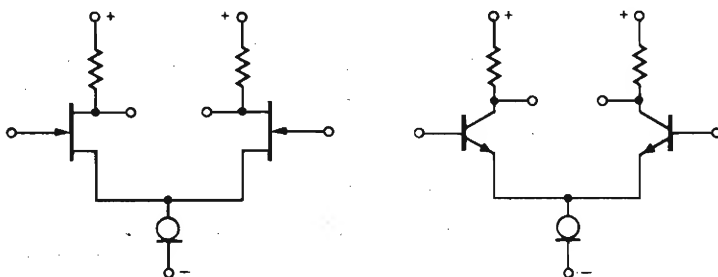
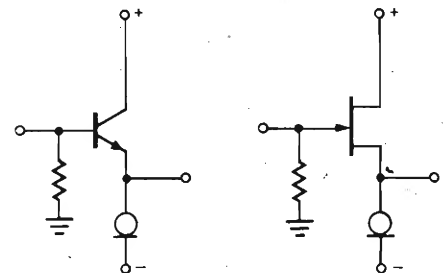
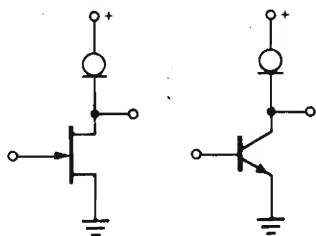
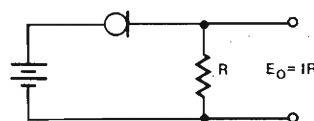



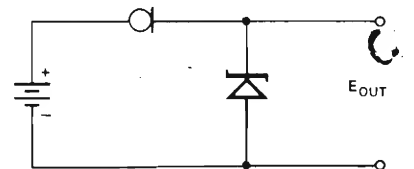
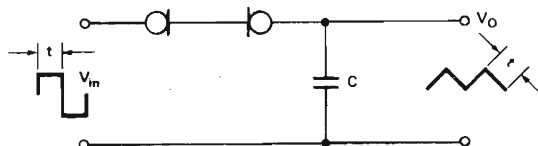
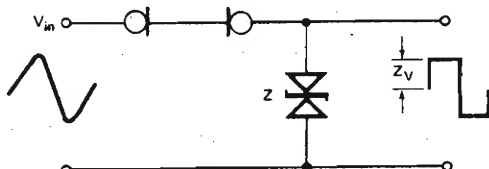
Fig. 7.

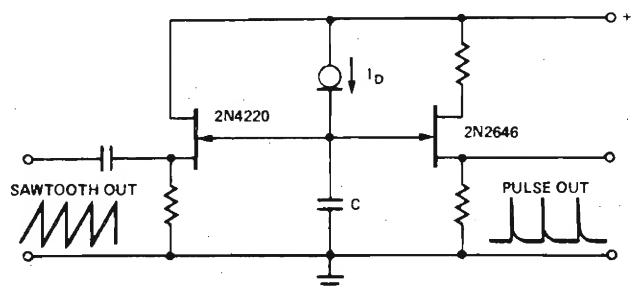
CURRENT SOURCE APPLICATIONS

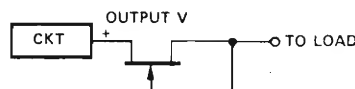
Note: o—⦶—o Represents any type configuration from Fig. 4-7.

DIFFERENTIAL AMPLIFIER CONSTANT CURRENT SUPPLY

EMITTER FOLLOWER OR SOURCE FOLLOWER

HIGH IMPEDANCE LOAD

LOW VOLTAGE REFERENCE

$E_O = IR$

BI-DIRECTIONAL LIMITER

ZENER DIODE SUPPLY FOR REFERENCE VOLTAGE

TRIANGULAR-WAVE GENERATOR

SAWTOOTH-WAVE GENERATOR: $t = \frac{CV_{FLD}}{I_D}$

SQUARE-WAVE GENERATOR

FET LIMITERS

The low "ON" resistance and current limiting features of the JFET makes short circuit protection easy. If normal drain current is 5 mA, a 2N4392 will drop approximately 250 mV but current limits at typically 50-60 mA. A 2N4303 or 2N3822 would have 30 mV drop at 100 μA, yet limit to 10 mA. The wide range of Teledyne devices offers a wide selection opportunity.

Sample-And-Hold Circuits

Sample-and-hold circuit design involves a series of difficult compromises, and keeping all of the variables and their effects sorted out can be troublesome. But a carefully tailored approach with the use of graphical aids can make the job a lot easier.

FUNCTION	SAMPLE	HOLD	RESET	V_0
	0	0	1	0
INPUTS	1	0	0	V_i
	0	1	0	V_i

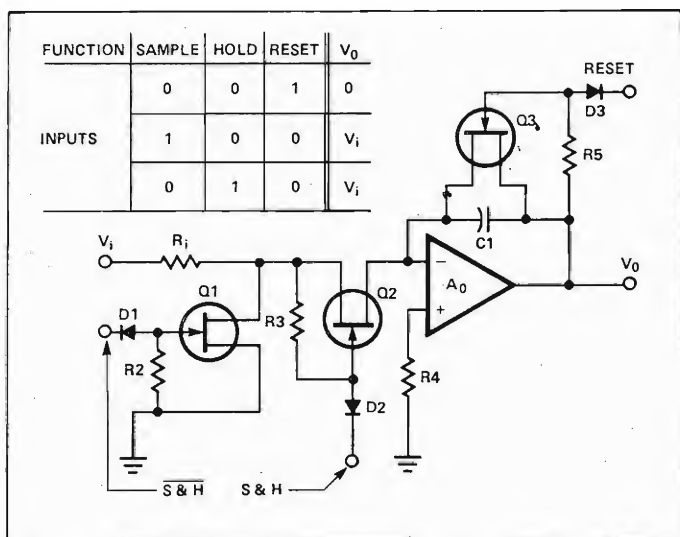



Fig. 1. A basic sample-and-hold circuit consists of an integrator circuit and FET switches. The FETs, Q1 and Q2, provide maximum isolation between the input and the stored signal. Transistor Q3 removes charge stored on capacitor C_I during reset. A truth table shows all possible input combinations.

A sample-and-hold circuit (Fig. 1) senses and stores the average value, over a simple interval, of a variable input signal. Three modes of operation — sample, hold and reset — must be carefully analyzed in the design. The characteristics of the switching circuit are also important. Of these four separate design problems, the hold mode (Fig. 2) is the most critical. This is because circuit operation and performance is committed for the longest time interval.

Assume, for our design example, that the range of the input voltage V_i must be 0.5 to 8 V, sample time t_s must be 13.5 ms, and hold time t_h must be 140 ms. The circuit must operate from 0 to 100°C and have a maximum sample error ε_s of 0.5% and maximum hold error ε_h of 0.75%. The sample error is defined as

$$\varepsilon_s = [-(V_i - V_o)/V_i] \times 100\%$$

and the hold error as

$$\varepsilon_h = \{[(V_o)_{t=0} - (V_o)_{t=140\ ms}]/(V_o)_{t=0}\} \times 100\%$$

Originally published as "Simplified Sample and Hold Design" in the September 30, 1971 issue of **Electronic Design** Magazine. Written by W. H. Williams of Westinghouse. Reprinted by permission.

Begin With The Hold Circuit

The primary concern in the hold mode is to ensure that the output drift rate remains within specified limits. Drift rate is defined as

$$\frac{dV_o}{dt} = \frac{I_{LT}}{C_I} \quad (1)$$

where dV_o/dt is the rate of change in output voltage time, $I_{LT} = V_o/R_{eq}$ is the op-amp bias current plus all leakage current, R_{eq} is the total equivalent leakable resistance and C_I is the integrating capacitor. Solving Eq. 1 for R_{eq} results in

$$R_{eq} = \frac{t_h}{C_I}\{\ln[(V_o)_{t>ts}/(V_o)_{t=ts}]\}^{-1} \quad (2)$$

where t represents an interval such that $t_s < t < t_h$. Resistance R_{eq} can also be expressed in terms of the components of Fig. 2:

$$R_{eq} = \frac{1}{\frac{2}{R_{L2}} + \frac{1}{R_{LC}} + \frac{1}{A_o r_i}} \quad (3)$$

where R_{L2} is the OFF resistance of each of two identical FET switches, R_{LC} is the leakage resistance of the integrating capacitor and $A_o r_i$ is the equivalent leakage resistance of the op amp.

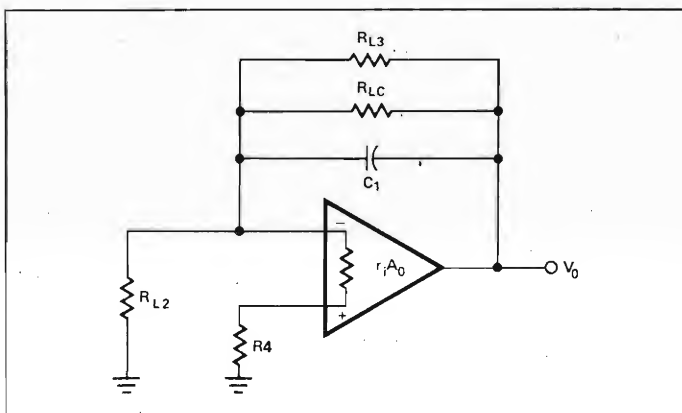



Fig. 2. The hold-mode equivalent circuit contains leakage paths through which C_I discharges during the hold mode. Resistor R_{L3} is the OFF resistance of Q2 and Q3, and R_{LC} is the leakage resistance of C_I. The resistances establish the rate at which the output voltage drifts.

Select The Op Amp

The selection of the op amp is now made on the basis of Eqs. 1-3. These expressions imply that an op amp with a low leakage current and high input impedance, such as the TOA7809, is needed to minimize drift rate.

Having selected the amplifier, we calculate the value of the integrating capacitor C_I by determining the maximum allowable drift rate that satisfies the design criteria. The

drift rate is affected by error sources inherent within the amplifier and dependent upon the circuit parameters. The major sources are the accuracy of integration, the offset voltage and current drifts with respect to temperature, and the power-supply rejection ratio.

The effects of these errors can be calculated from the known characteristics of the op amp and its feedback components. Other sources of error — such as the effects of drift vs time and system degradation as a function of component life — are not readily calculable. For these effects a worst-case condition of 15% over-design is assumed and ε_h is decreased from 0.75% to 0.65%.

Plot The Error Curves

A graph relating the calculable errors to a common normalized variable is shown in Fig. 3. The variable is the integration gain factor t_s/RC_I, where RC_I is the integrator time constant.

The curves are generated from component values and specifications obtained from the manufacturer on the components selected. All curves are plotted for an input integrating resistance in the range 1-10 kΩ.

The inaccuracy of integration (curve a) is approximated by the following expression:

$$\varepsilon_{in} \approx \frac{50\,(P+1)}{A}\left(\frac{t_s}{RC_I}\right)\ \% \qquad (4)$$

where $P = (R_o/R_I) + (R/R_{id}) + (R_oR/R_LR_{id})$, R_o is the amplifier output resistance, R_L is the load resistance, R is the integrating resistor, R_{id} is the amplifier differential input resistance and A is the open-loop gain of the op amp. The values for P and A are determined from the specification sheet on the particular amplifier selected.

The percent change in the output voltage as a function of the input offset voltage drifts and the input bias current drifts (curve b) is calculated as

$$\varepsilon_{Td} = \frac{(t_s/RC_I)\,(I_b\,R + V_{od}) + V_{od}}{V_i}\ \%/^\circ C \qquad (5)$$

where V_{od} is the drift rate in μV/°C. Curve d is Eq. 5 projected to 100°C.

The change in output voltage due to changes in supply voltage (curve c) is calculated as

$$\varepsilon_{PS} = \frac{PSRR}{(V_i)_{min}}\left(1 + \frac{t_s}{RC_I}\right)\ \% \qquad (6)$$

where PSRR is the power supply rejection ratio in μV/V.

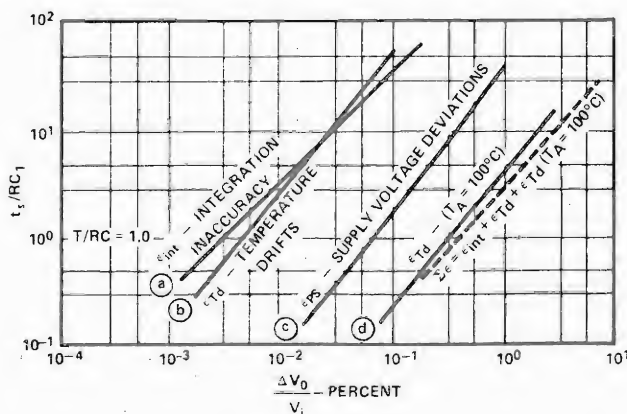



Fig. 3. Plotting the calculable errors from the op-amp specs and its feedback components leads to an isolation of each error, highlighting troublesome areas. The cumulative error is compared with the maximum allowable design error. A reasonable ratio of t_s/RC_I is then selected.

Use A Trial-And-Error Technique

A design value of $t_s/RC_I = 1$ is selected from Fig. 3 on the basis of the following considerations:

- for the specified input voltage range, increasing gain to improve low-level accuracy causes the output to become saturated at the high-level inputs;
- signal attenuation causes system-performance degradation for all levels of input and may contribute to circuit instability;
- the error for this ratio is negligible and
- checking circuit performance is practical and easy.

The allowable drift rate is easily calculated. Summing the errors for $t_s/RC_I = 1$ gives a total error of 0.37%. With a hold error of 0.65%, the allowable drift error $\varepsilon_d = (0.65 - 0.37) = 0.28\%$. The worst-case error occurs for $V_i = 0.5$ V, and during a time interval of 140 ms. Thus, the allowable drift rate is $dV_o/dt = (0.28)\,(0.5)/140 = 10.0$ mV/s.

For the calculation of C_I, current I_{LT} is determined for a worst-case temperature of 100°C. The FETs used are both 2N4092 types with a maximum leakage current of 20 nA (at 100°C). The maximum bias for the op amp is 10 nA, and the capacitor leakage is 5 nA. The value of capacitor C_I is calculated from Eq. 1: $C_I = [2(20) + 10+5]/10 = 5.5$ μF. The closest standard capacitor is 5.6 μF with 1% tolerance and −0.2% change over the temperature range.

With the op amp and integrating capacitor selected from hold-mode considerations, let's turn now to the design decisions determined by the sample mode, the reset mode and the switching circuit.

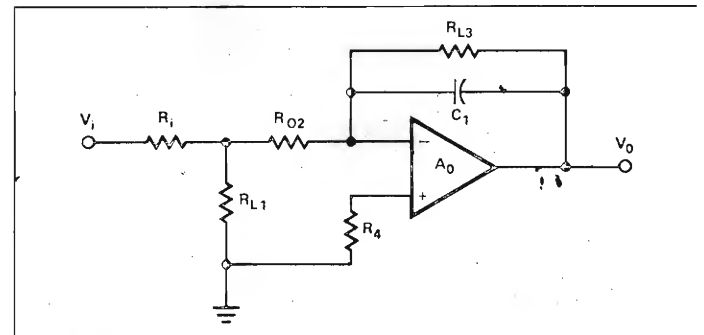



Fig. 4. The sample-mode equivalent circuit design requires $R_O << R_i << R_{LI}$. This results in minimum attenuation of the input voltage and achieves a further reduction of the integration error.

Check The Sample Mode

An equivalent circuit representing the sample mode is shown in Fig. 4. From this equivalent the input resistance R_i — a fixed and variable resistance — is calculated. Since the error caused by the integrator is negligible, the integrator output is described by the ideal case: $V_o = V\,(t_s/RC_I)$, where $R = R_i + R_{LI}$, and $R_{LI} = 30$ Ω, the leakage resistance of the FET. The integration gain constant $t_s/RC_I = 1$ and $R_i = 13.5/5.6 = 2.41$ kΩ. A convenient form for R_i is a 2.32 kΩ fixed resistance and a 200 Ω potentiometer in series. Assuming initial adjustments within ±0.05% the deviations of output voltage from initial adjustments range from 0.3% to 0.6% over the temperature range.

The equivalent circuit for the reset mode is shown in Fig. 5. This mode of operation normally places the amplifier in a potentially unstable state, because the input resistance is very large and the resistance in the feedback path has been made very small. However, since the actual input signal is being attenuated, the circuit configuratior

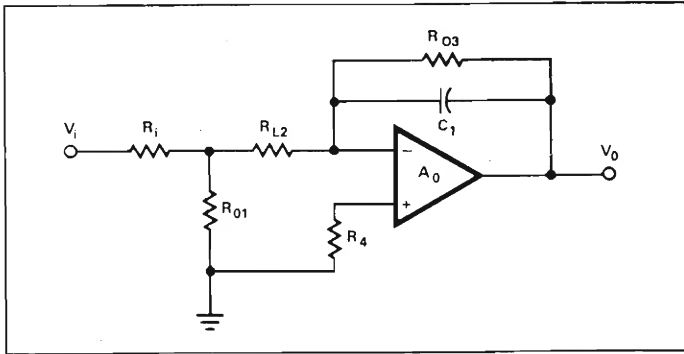



Fig. 5. The reset-mode equivalent circuit applies during discharge of C_i. The input voltage is attenuated by R_{0i}, where $R_{0i} << R_i$, and isolated by R_{L2}. Unity gain compensation eliminates instability.

becomes that of a voltage follower and, with unity gain compensation, it remains stable during reset.

The Switching Circuit Is Important, Too

Another important factor in this design is the switching circuit, especially at the input. A design consideration is that semiconductor switches do not exhibit the ideal zero ON resistance nor infinite OFF resistance. And the bias voltage must be selected to ensure turn-on and turn-off at the correct times.

The finite resistances of the FETs cause voltage errors. However, with the components selected, a typical value for this error is about 0.0005% in the initial amplitude of the output. For the hold mode this tends to aid rather than degrade performance.

A more important consideration is ensuring the correct turn-on and turn-off times. The ON condition for a FET exists when $(V_i)_{max} \geq V_{EE}\text{-}V_{RD}$, where V_{EE} is a positive gate voltage and V_{RD} is the voltage required to keep the gate diode reverse-biased — normally about 50 mV.

For the OFF condition, the relation to be satisfied is $(V_i)_{min} \leq V_{CC}\text{-}V_{FD}\text{-}V_p$, where V_{CC} is a negative gate voltage,

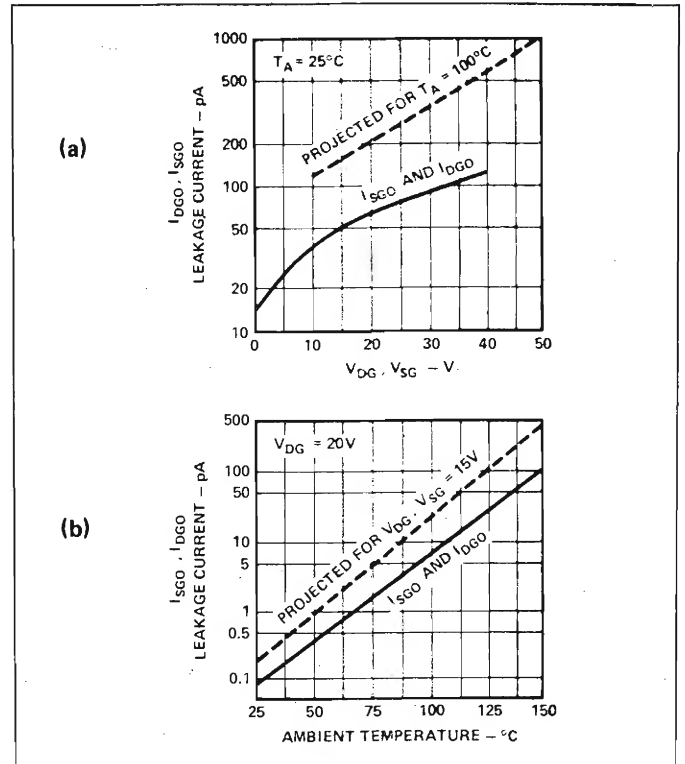



Fig. 6. The FET leakage parameter I_{DGO} which has a marked dependence on voltage (a) and temperature (b) is used to determine $(R_{L1})_{min}$ or $(R_{L2})_{min}$.

V_{FD} is the forward-voltage drop of the gate diode and V_p is the pinch-off voltage. For the FETs selected, $V_{RD} = 0.05$ V $V_{FD} = 0.6$ V and $V_p = 7.0$ V. The required gate voltages with $0 \text{ V} \leq V_i \leq 8.0$ V, are $V_{EE} \geq 8.05$ V and $V_{CC} \leq -7.6$ V The respective voltages selected are +15 V and −15 V.

The equivalent leakage resistance R_{eq} (see Eq. 3) is now calculated from the leakage parameters of the FETs. This calculation is important because it represents the leakage path for current while in the hold mode.

In the hold mode, the leakage path between the drain and gate is significant. To determine the minimum value of

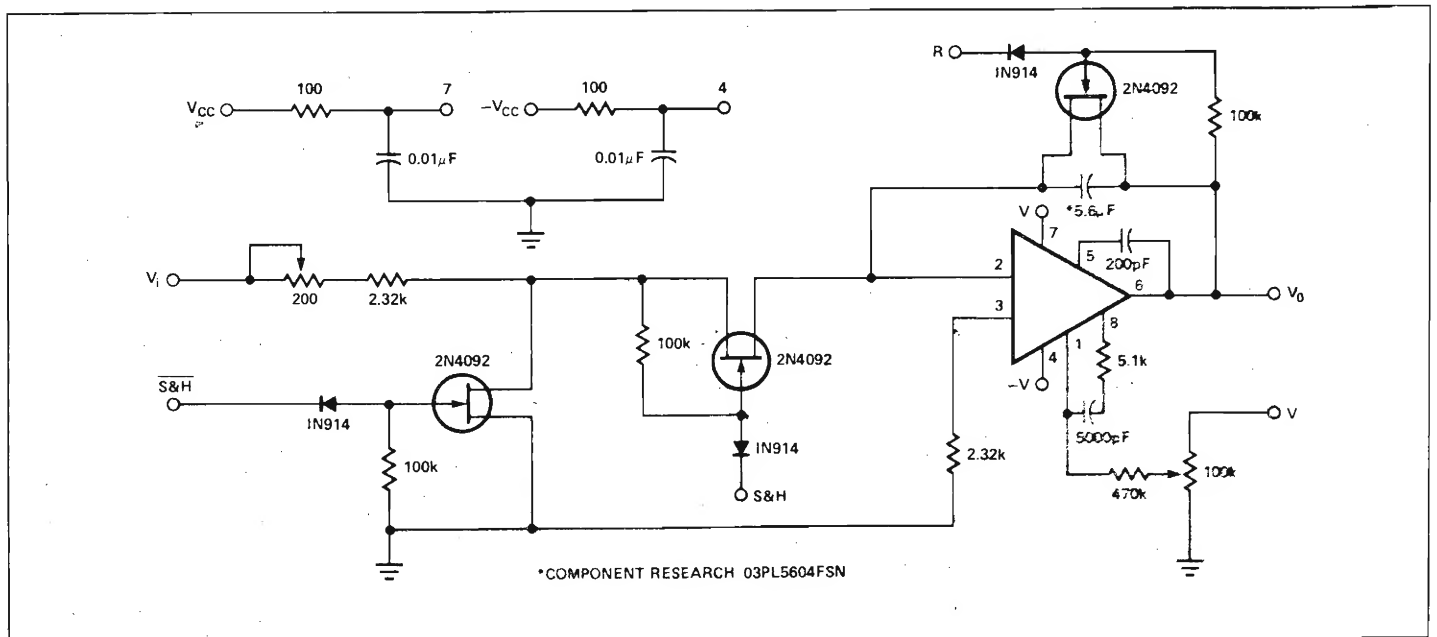



Fig. 7. The final sample-and-hold circuit design includes all of the components selected, biasing for the FET switches, the compensation network and the output of the op amp set adjustment. The adverse effects of worst cases are compensated for by an over design technique.

this resistance (R_{L1} or R_{L2}) consider the curve shown in Fig. 6a. The value of I_{DGO}, the drain-to-gate leakage with the source open, for V_{DG} equal to −15 V is approximately 50 pA or .05 nA. This value of I_{DGO} is projected to the 25°C point on the curve of Fig. 6b.

Since the gate leakage current vs temperature is linear, the value of I_{DGO} may be extrapolated to the 100°C point for the worst-case. Thus, I_{DGO} at 100°C is approximately 3.5 nA. However, the maximum value of I_{DGO} for $V_{DG} = 20$ V is 0.2 nA from the specification sheet for the 2N4092 transistor.

Projecting this point on to the curve in Fig. 6b, and extrapolating to the 100°C point, the maximum value of I_{DGO} for $V_{DG} = 15$ V is found to be approximately 20 nA. The minimum value of R_{L1} or R_{L2} in the integrator circuit is calculated: $R_{L1} = R_{L2} = V_{DG}/I_{DGO} = 750$ MΩ. The equivalent leakage resistance is, from Eq. 3, $R_{eq} = 1/[2/750\times10^6 + 1/16\times10^{10} + 1/540\times10^6] = 221$ MΩ.

The basic sample-and-hold circuit design is now complete, with the final schematic as shown in Fig. 7. Graphs of measured data for the circuit are shown in Fig. 8. The test data show circuit accuracy in duplicating the input signal amplitude and the accuracy in holding this amplitude for a specified period of time. Drift rates for different amplitudes of output over the temperature range for steady-state non-switching conditions are shown in Fig. 8a. Figures 8b and 8c show circuit performance over the temperature range 0-100°C for switched conditions. Except for the region below 1.0 V, the amplitude is reproduced to an accuracy of 0.25% while the droop is held to 0.1%.

Added Teledyne Note:

Although the leakage figures used by Mr. Williams should be adequate, tighter leakage selections at nominal extra cost are available from Teledyne Semiconductor.

Th 2N4092 is a general purpose FET. It is available in epoxy as the U1898E. Within the same family, 30 ohm max or $V_{GS(OFF)}$ 3 V max is available. For tighter r_{DS} requirements, the 2N4977 with 15 ohms max or the 2N5432 with 5 ohms max is available.

Popularly used in many DVMs for sample-hold circuits, are the 2N4416, U1994E (epoxy 2N4416), and 2N3823, 4.

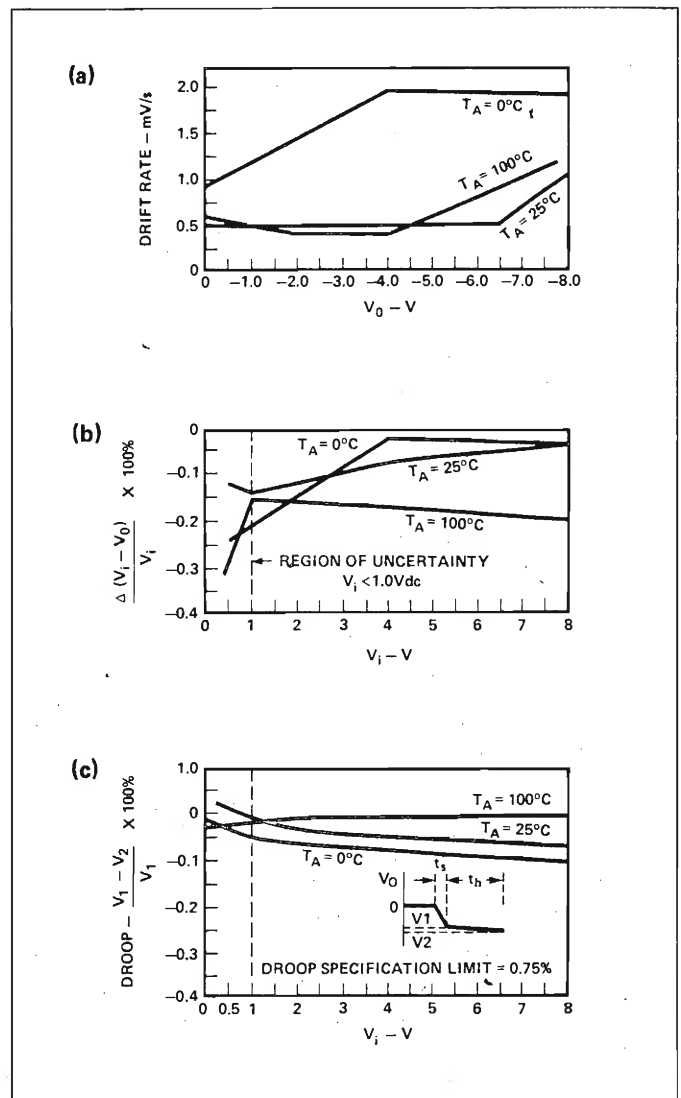



Fig. 8. Measured data of the sample-and-hold design show the drift rate (a) plotted for one-second averages. Drift rates are significantly smaller for $t_h << 1$s. The accuracy with which a given input is reproduced at the output is shown in b. Plotted in c, the percent change in the output voltage

FET Oscillators

Higher frequency FETs at bi-polar type prices make these devices attractive for RF applications. The designer is not limited by input impedance or greatly varying capacitances as a function of operating temperature. Circuit design is identical to vacuum tube triodes, and close to that of bi-polars. Design factors to consider are frequency stability, starting conditions, and power output (a function of biasing current).

Oscillator Classes

Most common are the active amplifier types using frequency selective feedback in proper phase and amplitude to sustain oscillator unity input gate-output network gain at 360° phase shift. The oscillator may have tuned circuits in both input and output.

1. **Colpitts Oscillator** — Utilizes a capacitive divider in the parallel LC tank circuit between FET amplifier's input and output terminals with a tap to the amplifier's common terminal. This is the cheapest and most popular method. See Fig. 1.

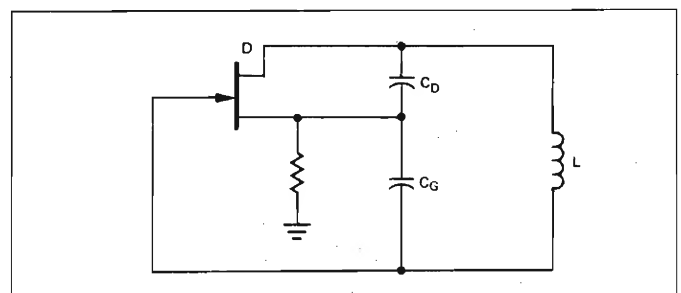



Fig. 1. Colpitts

2. **Hartley Oscillator** — Similar to the Colpitts except featuring an inductive divider. The inductances tune with the drain-gate feedback capacitance to fix frequency. See Fig. 2.

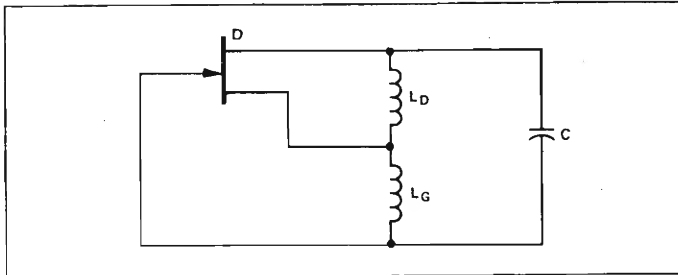



Fig. 2. Hartley

3. **Crystal Oscillator** — Where frequency stability is particularly critical, the crystal replaces the tuned circuit. Over temperature, this method provides 5-10 times better temperature stability. See Fig. 3.

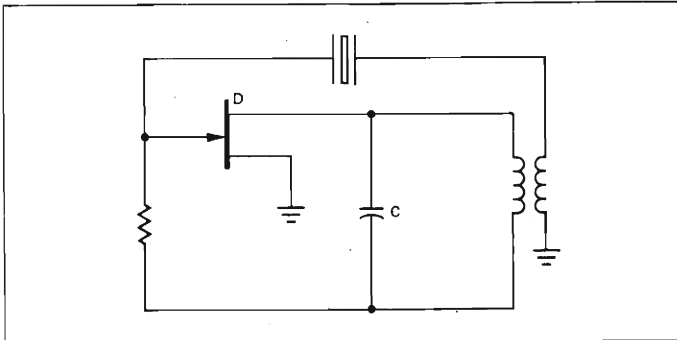



Fig. 3. Crystal

Frequency Stability

Since FET capacitances are predictable reversed-biased junctions, the mistuning due to operating current and temperature shifts is slight. The bi-polar transistor circuit mistuning shifts arise from the forward-biased emmitter-base junction which is almost proportional to emitter current which changes with temperature. Biasing techniques in the FETs minimize the capacitance changes. As a comparison, a 100 MHz typical FET oscillator, Fig. 4, would have 20-25% of the frequency shift over 100°C temperature variation compared to a bi-polar oscillator.

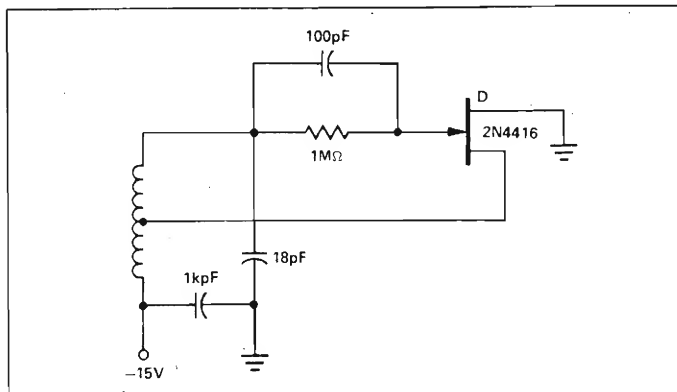



Fig. 4. 100 MHz Oscillator

Starting Conditions

The feedback factor (gain) of the feedback network is:

$$B = \frac{Efb}{Eo} \left(\begin{array}{l} \text{Efb—tank input feedback voltage} \\ \text{Eo—output voltage from output tank} \end{array} \right)$$

and the amplifier gain

$$K = \frac{Eo}{Efb} \text{ or } K = \frac{1}{\beta} \qquad \begin{array}{l} \beta = Cd/Cg \text{ (Colpitts)} \\ \beta = Lg/Ld \text{ (Hartley)} \end{array}$$

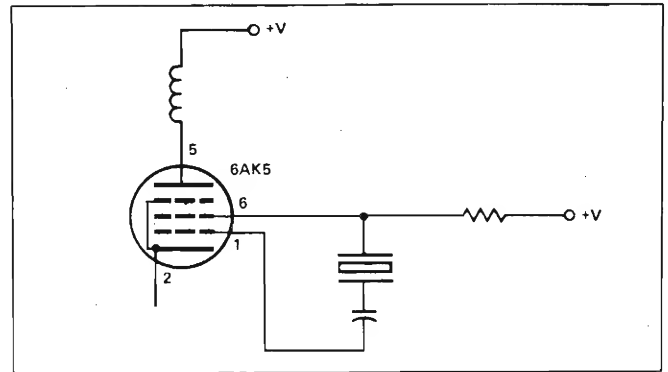



Fig. 5. Vacuum tube pentode crystal oscillator

In a few cases, a vacuum tube pentode doubles as a oscillator/amplifier circuit, as shown in Fig. 5. Circuit-wise the screen grid is acting as the plate of a triode. The standard amplifier FETRON replacement leaves the screen gri connection open — fine for standard amplifier circuits.

To simulate the action of the screen grid and provid temperature compensation, a TS6AK5 OSC FETRON wa developed to simulate the action of the pentode scree grid. Internal wiring features a parallel combination re sistor/capacitor between the screen grid and plate pins In a crystal oscillator as in Fig. 6, it is important to hol crystal current constant to prevent frequency shifts.

For oscillation to start, the loop gain must be greate than one, or:

$$AB \geq 1 \text{ where } A = YfsZt \qquad Zt \text{ — tank impedance}$$

Therefore, for oscillations to start:

$$Yfs > \frac{Cg}{CdZt} \text{ (Colpitts)} \qquad Yfs > \frac{Ld}{LgZt} \text{ (Hartley)}$$

Oscillators such as shown in Fig. 4 operate a zero-ga bias when initially turned on. Therefore, utilizing 2N4416 c U1994E provide Yfs > 4500 μmhos starting transconduc ance. The minimum guaranteed 5 mA I_{DSS} and 30 V V(BF Gss provides adequate power output for most application

Power Output

Besides the circuit's tank efficiency, N, the oscillatic amplitude is limited by FET I_{DSS}, supply voltage or devic max V(BR) Gss, and FET gain near Yfs UHF roll-off. Pow output is approximately give by:

$$Pout = \frac{e_i^2 N}{R_L'} \qquad \begin{array}{l} e_i = \text{forms square wave voltage} \\ R_L = \text{transformed load impedance} \end{array}$$

Practically in a 2N4416, this will mean 5-25 mW Pout.

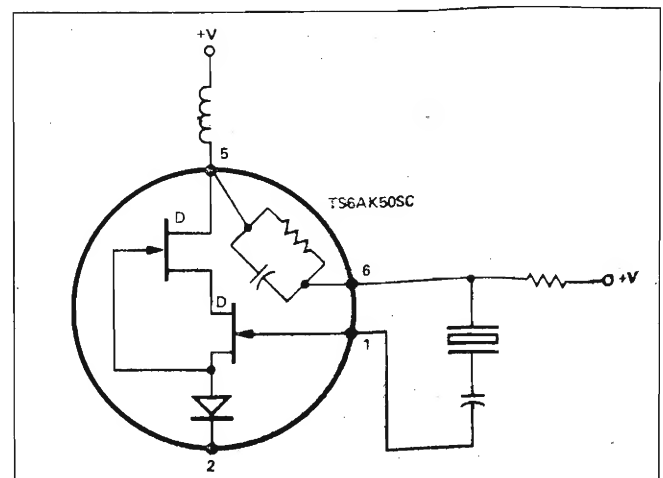



Fig. 6. FETRON replacement for 6 AK5 in Fig. 5 circuit

FETRON Considerations

Most present vacuum tube oscillator circuitry utilizes either the Colpitts, Hartley or Crystal oscillator in conjunction with a vacuum tube triode. In these situations, the standard FETRON (solid-state vacuum tube replacement) twin triode can be used.

Dual FET Applications

INTRODUCTION

With the advent of high impedance transducers and other high impedance signal sources, a critical need for FET Duals exists. Application areas such as preamplifiers, operational amplifiers, oscilloscope front ends, multiplexers and electrometers dictate 10^6 to 10^{13} ohm input impedance. Some new monolithic op amps available have 1 nA input current. However, the slew rates are in the area of 0.01 V/μsec. To get up to a relatively slow 0.5 V/μsec, the input current zooms to 20-30 nA. Utilizing Dual FETs, slew rates of 100-1000 V/μsec are easily obtained, with no input current compromise.

OPERATION

Junction Dual FET circuitry is the same as found in bipolar differential amplifiers. However, distinct differences occur in the 25°C and temperature tracking of the FET Gate-Source Differential Voltage versus the Bi-polar Base-Emitter Differential. A bi-polar dual will track approximately 2-2.5 μV/°C/mV $V_{BE\ 1-2}$. This performance is independent of emitter current from less than 1 μA to more than 1 mA.

The temperature track of an FET may be up to 250 μV/°C even if the room temperature match is within a few millivolts. Dual FET manufacturers are able to obtain 5-10 μV/°C tracking performance through the use of exotic computerized matching of discrete chips, or Teledyne Semiconductor's interlaced, diffusion isolated, monolithic dual FET comprising the SU2365-9, A, series. In spite of the specialized matching techniques, the discrete pair matching is very much a function of drain current. For guaranteed performance, the data sheet matching current conditions must be used. Typical normalized curves relating Gate-Source match and track as a function of drain current are included in all Teledyne Semiconductor dual FET data sheets. (See example of SU2365-9, A, in Figure 1.)

Fig. 1. Gate-Source Tracking

JFET DIFFERENTIAL AMPLIFIER CIRCUITS

Dual FET's can be used in all the ways bipolars are presently used plus several unique ways that use features of JFET's to advantage. A few of the typical circuits are shown below.

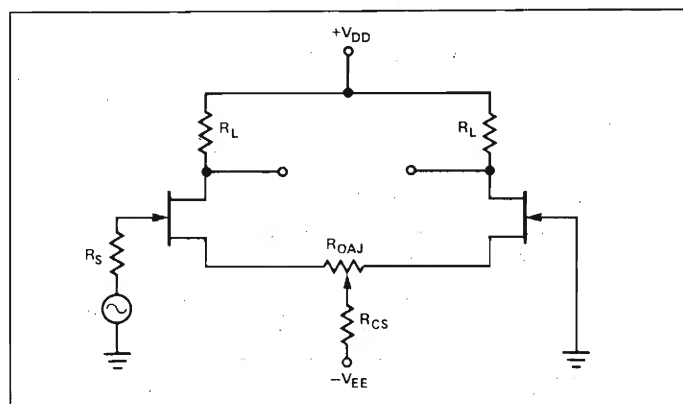



Fig. 2. Differential Amp With Gain

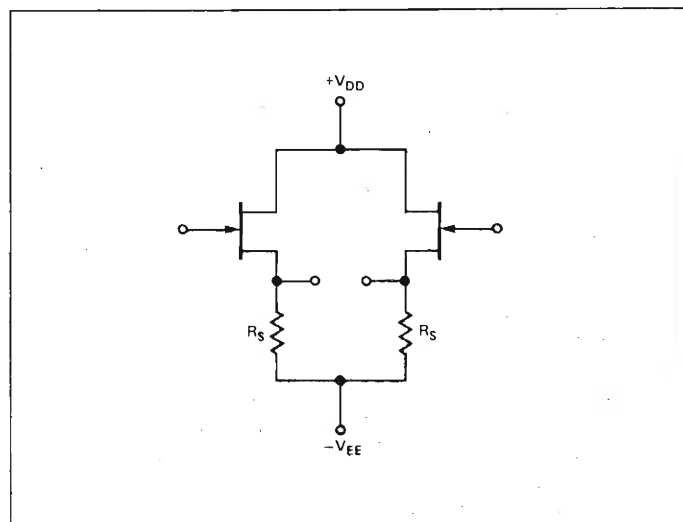



Fig. 3. Source Follower Diff. Amp

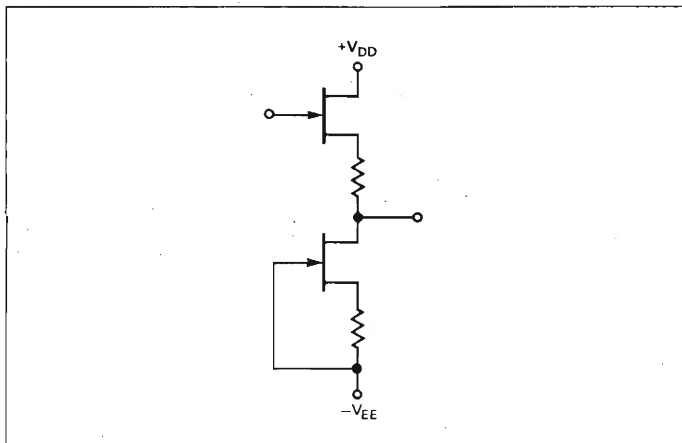



Fig. 4. Temp Compensated Single Input Amplifier

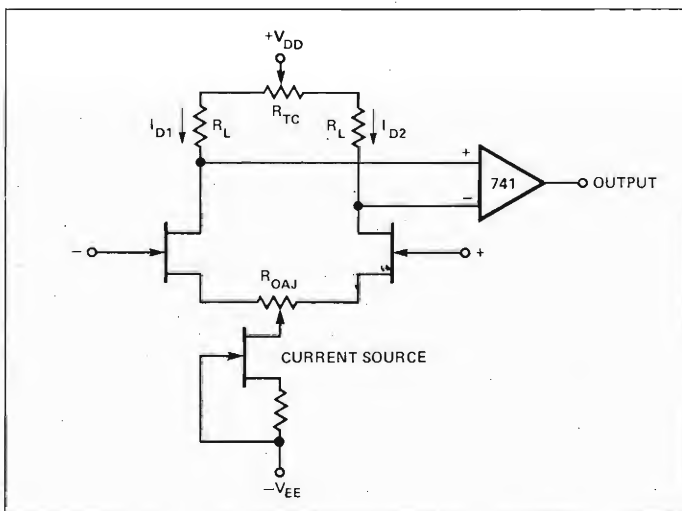



Fig. 5. FET Op Amp featuring Offset Voltage Adjustment, Temperature Coefficient Adjustment, and FET Current Source.

Most common usage applications do not require the temperature compensation shown in Figure 5. If the application requires less than 25 $\mu V/^\circ C$, it is cheaper to buy a unit with less than 10-20 $\mu V/^\circ C$ than it would to use a 100 $\mu V/^\circ C$ unit and trim out thermal effects. If the compensating resistor R_{TC} is necessary, the change will be approximately 4-5 $\mu V/^\circ C/\mu A$ of $I_{D1} - I_{D2}$. Of course, the exact trimming would be defined by trial and error. For a typical 10 kohm R_L, a 500 ohm R_{TC} should be adequate.

CURRENT SOURCES

Although the Common Mode Rejection Ratio, CMRR, of the Dual FET may be high, the circuit CMRR will deteriorate if the current source is poor. Using Figure 2 for analysis, the voltage gain of the FET differential amplifier, "A_{dd}," if both sides are matched is: $A_{dd} = \frac{Yfs\,R_L}{1+Yos\,R_L}$

and normally $Yos\,R_L << 1$

or $A_{dd} = Yfs\,R_L$

the circuit common mode gain, "A_{CC}," is

$$A_{CC} = \frac{Yfs\,R_L}{1+YosR_L+2Rcs\,(Yos+Yfs)}$$

and normally $YosR_L << Yfs$

$2\,RcsYfs >> 1$

or $A_{CC} = \frac{R_L}{2\,Rcs}$

By definition, circuit CMRR $= \frac{A_{dd}}{A_{CC}} = 2Yfs\,Rcs$

Thus we can see the importance of Rcs, whether it is the simple resistor or a complex circuit.

Several of the alternative current sources are shown in Figs. 6-9 using the nominal 400 μA to supply 200 μA per side.

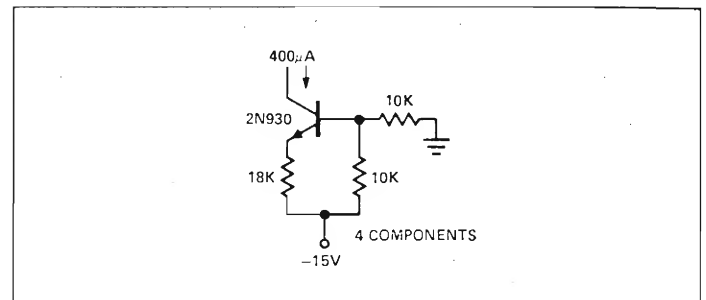



Fig. 6. Uncompensated Bipolar CS

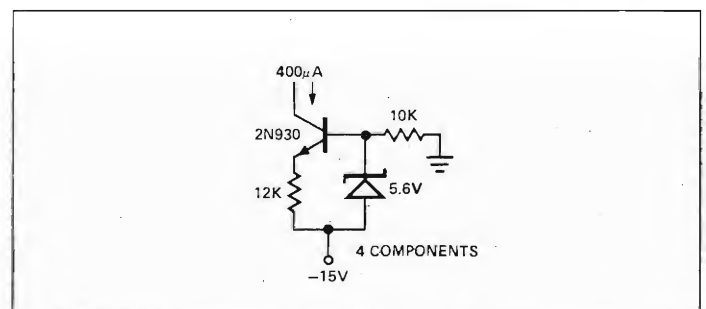



Fig. 7. Temperature Compensated Bipolar CS

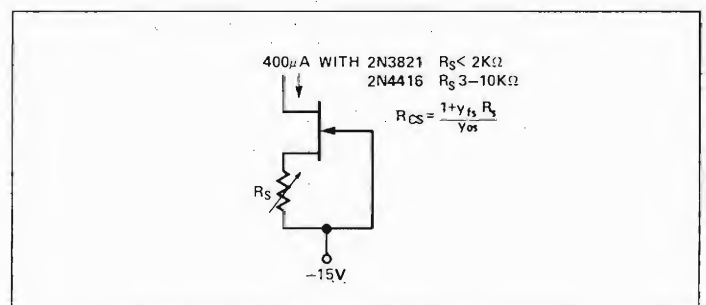



Fig. 8. FET Current Source (2 Components)

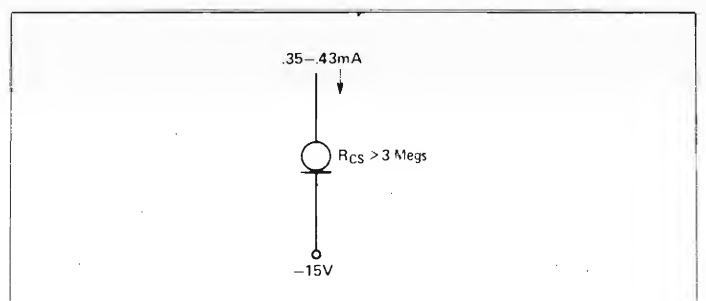



Fig. 9. Teledyne TCR5288 (1 Component - 2 Leads)

SPECIFYING DUAL FETs

Many of the older specifications of Dual FETs still in prin are the result of non-meaningful "specmanship". Even though only seven or eight parameters are critical, many specs have, in addition to the standard guaranteed parameters, several meant to box out competition and/or reflec something done in device matching. These parameters result in higher user cost and, often, slow delivery. The following discussions represent a common sense way to

select one of the many duals available and insure desired performance at minimum cost.

A. Desirable features:
1. High Input Impedance — low I_G
2. Low Gate-Source differential match — 25°C and over temperature
3. Stable drift over varying drain current
4. Drift linear with temperature
5. High Common Mode Rejection Ratio — CMRR
6. Adequate transadmittance — Yfs
7. Low Noise Figure
8. High Common-Mode Range

B. Important Parameters — (SU2365A-9A as Evaluation Vehicle)
1. I_G — This maximum specification which is given at both 25°C and an elevated temperature, tells the designer the maximum V_{GS} offset he can expect across his source impedance. When used with one input grounded, this dominates. When matched gate resistance exists, then I_{G1-2} is important. Note: I_G and I_{G1-2} double every 11-12°C. (Referring to Fig. 10)
$V_{GS\ ERROR} = I_G \times R_G$
Worst case, $I_{G\ MAX} = 0.5$ nA at 80°C
and $V_{GS\ ERROR} = 50\ \mu V$ (equiv. 1 $\mu V/°C$)
If $R_g = 500k$ ohms
$V_{GS\ ERROR} = 250\ \mu V$ (equiv. 5 $\mu V/°C$)
Gate leakage does affect the i_n component in noise figure where $N_F = 10 \log \left[\frac{1+(V_n + i_n\ Rs)^2}{4KTRs}\right]$
NOTE: I_{GSS} is really meaningless in dual operation. At 50% of $V_{(BR)GSS}$, I_G may go into nA's where I_{GSS} will stay in low pA's.

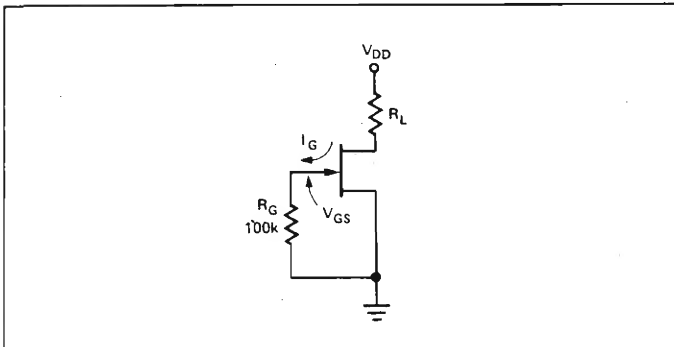



Fig. 10. Gate Leakage I_G

2. I_{G1-2} — This maximum matching spec determines the differential error when both inputs have high gate resistance.
If $I_{G1} = 0.5$ nA at 80°C
$I_{G2} = 0.2$ nA at 80°C
$R_{G1} = R_{G2} = 500K$ ohms
Then $V_{GS1-2} = I_{G1}R_{G1} - I_{G2}R_{G2}$
and $V_{GS1-2\ ERROR} = 150\ \mu V$
(equiv. 3 $\mu V/°C$)
3. Yfs½ (at I_D,V_{DG}) — It is important this matching value be at the drain current of the other key parameters. It is a major parameter contributing to Common Mode Rejection Ratio, CMRR, and affects the circuit gain matching by the familiar equation previously discussed.
$$Add = Yfs\ R_L$$
In a source follower, the effect is negligible.

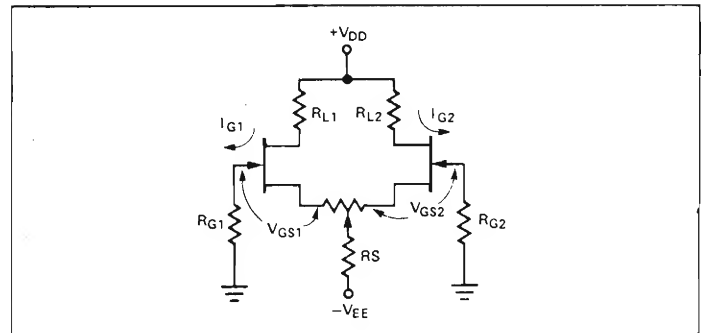



Fig. 11. Balanced Dual Circuit

4. Yfs (at I_D) — As discussed in Yfs½, Yfs at the operating current I_D (not I_{DSS}), multiplied by the effective load resistance equals the circuit gain. Most designers don't object to more gain, or in the case of a source follower, closer to unity gain:
$$A_{V\ SF} = \frac{Yfs\ Rs}{1+YfsRs}$$
When YfsRs >> 1, $A_{V\ SF} = 1.0$
5. CMRR — This specification, only important when volts rather than mV swings at the input of the circuit is involved, could override other drift parameters. The common Dual FET definition is $CMRR = 20 \log \frac{\Delta V_{DG}}{\Delta V_{GS1-2}}$. With a good current source, ΔV_{DG} follows ΔV_{GS} at the input.
To realize this parameter's importance, take the circuit where the input voltage is ±5V.

DEVICE CMRR	$V_{GS1-2\ ERROR}$
60 dB	10 mV
80 dB	1.0 mV
100 dB	100 μV

of course, Vin ±0.5 V, CMRR = 80 dB,
$V_{GS1-2\ ERROR} = 100\ \mu V$
6. $|V_{GS1} - V_{GS2}|$ (at I_D, V_{DG}) — This represents the 25°C gate differential offset error initially present. This error is easy to zero out, but as the resistor value grows, so does the potential error due to resistor temperature coefficients.
NOTE: The normal differential amplifier operates grounded gate. Consequently, V_{DG} is the independent fixed by $V_{DD} - I_D \cdot R_L$. V_{DS} is the dependent variable varying according to the positive source voltage. As such a $V_{DG} = 10$ V may be $V_{DS} = 7$ V. Unfortunately, some incorrect specs carry over the V_{DS} condition analogous to V_{CE}. Bi-polar V_{BE} varies only 10-15 mV in a large lot versus 2-3 volts on FET V_{GS}.
7. $\frac{\Delta |V_{GS1} - V_{GS2}|}{T_A}$ — Dictates what maximum drift one can expect from Dual over temperature at the specified I_D current. Don't expect 100% yield operating at 300 μA if the spec says 200 μA — odds are excellent on SU2365-9 series, however.

B. Necessary Parameters — Minor Importance
1. $V_{(BR)GSS}$ — Although the device is not operated in this mode, it does indicate potential danger areas. Remember I_G and study the vendors' curves, e.g. If $V_{DGnd} = +15$ V and $V_{GGnd} = \pm 5$ V
then, $V_{DG} = +10$ to $+20$ V
2. $V_{GS(OFF)}$ — Although not directly used in the circuit,

this spec combined with I_{DSS}, gives the user some indication of his operating gate-source voltage, and the limits of his peak positive input voltage. The family curves on the SU2365 series indicate satisfactory operation when $V_{DG} \geq 1.0\text{-}1.5$ V:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$\text{or } V_{GS(operating)} = V_{GS(OFF)}\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

3. Yos (at I_D) — Output Admittance is of real importance only when Yos R_L is not << 1. For example, a typical R_L equals 10 or 20K ohms. With Yos < 2 μmhos, the maximum error could be 4% in "A_{dd}." Anything lower is insignificant, even 5 μmhos with R_L = 20K ohms is only 10% gain reduction — device to device Yfs varies that much.

$$A_{dd} = \frac{Yfs\, R_L}{1 + Yos R_L}$$

Yos is a function of voltage where a Yos < 5 μmhos at V_{DS} = 20 V, I_D = 20 μA usually corresponds to Yos < 13-15 μmhos at V_{DG} = 10 V, I_D = 200 μA. It is easy to specify unnecessarily tight values that do nothing for circuit performance. The parameter is one of many contributors to CMRR.

4. Yos_{1-2} — Parameter will influence differential gain as indicated in the Yos at I_D discussion. A Yos_{1-2} < 2 μmhos with R_L = 20K ohms affects gain by a couple of percent. It is a contributor to CMRR. As such, the presence of CMRR, eliminates the Yos_{1-2} requirement.

5. N_F, Vn — One of the two parameters should be specified. N_F in dB is a function of R_G and as such, may be non-meaningful in the circuit application. Given Vn (e_n), one can approximate the noise figure for any gate resistance — "i_n" being of negligible affect until R_G > 10 Megohm. Don't be snowed by thinking a N_F < 0.5 dB at R_G = 10 MΩ is any better than < 1 dB at R_G = 1 MΩ or e_n < 50 nV/$\sqrt{\text{Hz}}$.

6. Ciss, Crss — These parameters become important only in MHz operation, particularly when used in a temperature compensated video amplifier application, (i.e., front end of an oscilloscope). Usually in these situations, a 2 mA, 5 mA or 10 mA match type current-matched dual is used. In most cases, for normal op amp application, a few pF are of little concern to the designer.

7. $V_{(BR)}G_1G_2$ — Gate-To-Gate breakdown never is a problem on a non-monolithic two chip Dual FET. However, in some monolithic duals, there is a common back gate resulting in breakdowns of 5-6 V. This is overcome by extra circuit biasing of the substrate. The SU2365-9 series guarantees 30 V minimum and typically is 80 V. It features a complete device-to-device PNP type isolation technique.

C. Meaningless Parameters

Many old device specs contain parameters that reflect a peculiar manufacturing method or lack of circuit knowledge. Sometimes their purpose is to prevent or limit second sourcing.

1. Yfs½, I_{DSS}½ (at V_{GS} = 0) — Normally the device is operated at a specific current where the other key parameters are stated. The design value is negligible.

2. Yfs (at V_{GS} = 0) — JEDEC 2N numbers require a min./max., however, it should be loosely speced. The real gain results from the operating point value. A Yfs at V_{GS} = 0 of 3 mmhos versus 4 mmhos at the same I_{DSS} will make a difference of only 50-150μmhos at I_D = 200 μA.

$$Yfs_{I_D} = Yfs_{V_{GS}=0}\left(1 - \frac{V_{GS}}{V_{GS(OFF)}}\right)$$

$$\text{or } Yfs_{V_{GS}=0}\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

3. V_{GS}(F) — A JFET is a voltage controlled high input impedance device. This parameter is meaningless.

4. Tight I_{DSS}, gm Specs — Except for single ended amplifier applications, (Fig. 4), Duals operate at constant current, eliminating variations which would otherwise be present in resistive source biasing.

D. Voltage Choice

Teledyne Semiconductor has standardized V_{DG} in the dual series at 10 Volts. Also common is V_{DG} = 15 V. Popular is V_{DD} = +15 V, I_D = 200 μA, R_L = 20 kΩ. Under this condition with zero input, V_{DG} = +11 V. V_{DS} = +20 spec is far from practical. It should be noted that lower voltage operation is practical.

COMPARATIVE SPECIFICATIONS

To get a feel for spec variations, the 2N3954, 2N5197, and SU2365A are compared in Table 1. Obviously, the 2N5197 and SU2365A provide the designer with far more pertinent information than the older 2N3954. Coding is used to indicate advantage (+), not important (o), disadvantage (−).

CAUTION

In an effort to make specifications attractive, and yet not overpriced, general spec parameters, conditions, and limits usually reflect what is necessary for wide general customer acceptance. Periodically, tightened parameter specifications will be needed for an application. Teledyne encourages inquiries to optimize requirements in these cases.

Don't write a specification where a 20% yield on each of three parameters will result in 1% overall yield. If you need I_G <1 pA maximum don't try to squeeze it out of the SU2365A when you can go to the TD5902-9 series, sacrificing on Yfs but getting the standard 1 pA max.

If your differential input signal is a few millivolts, don't pay extra for CMRR >100 dB. If leakage is of minor concern, buy the SU2365, rather than the "A" version. Chances are that by letting the manufacturer evaluate your exact requirements after doing your homework, the final spec if not one of the *good standard devices* available, will insure modest price, good delivery and second sourcing.

Test Specification	Units	SU2365A	2N5197	2N3954
$V_{(BR)GSS}$ @ 1 μA	V	>30	>50 (+)	>50 (+)
$-V_{GS(OFF)}$ @ V_{DS} = 15, 20 V I_D = 1 nA	V	<3.5 (o)	.7-4.5	1-4.5
$-V_{GS}$ @ V_{DG} = 15, 20 V I_D = 200 μA	V	<2.5 (+)	0.2-3.8	0.5-4
I_G @ V_{DG} = 15, 20 V I_D = 200 μA	pA	<20	<15	<50 (−)
I_{DSS} @ V_{DS} = 10 V, 20 V V_{GS} = 0	mA	0.5-10	0.7-7	0.5-5
Yfs @ V_{DG} = 15, 20 V I_D = 200 μA	mV	1-2 (+)	0.7-1.5	No Spec (−)
Yfs @ V_{DS} = 10, 20 V V_{GS} = 0	mV	>1.5	1-4	1-3 (−)
Yos @ V_{DG} = 15, 20 V I_D = 200 μA	μV	<2	<4	No Spec (−)
Yos @ V_{DS} = 20 V V_{GS} = 0	μV	No Spec	<50	<35
Yos_{1-2} @ V_{DG} = 20 V I_D = 200 μA	μV	No Spec	1 (o)	No Spec
CMRR @ V_{DG} = 10-20 V I_D = 200 μA	dB	>90 (+)	No Spec	No Spec
Ciss @ V_{DS} = 20 V I_D = 200 μA	pF	16 pF	6 pF	4 pF (o)
Yfs½ @ V_{DG} = 15, 20 V I_D = 200 μA	—	.95-1.0	.97-1.0	.97-1.0
I_{G1-2} @ V_{DG} = 12, 20 V I_D = 200 μA, 100°C	nA	0.5 (+)	<1	<2
V_{GS1-2} @ V_{DG} = 10, 20 V I_D = 200 μA	mV	<5	<5	<5
V_{GS1-2} @ V_{DG} = 10, 20 V I_D = 200 μA	μV/°C	<10	<10	<10
I_{DSS}½ @ 20 V	—	No Spec (o)	.95-1.0	.95-1.0
$V_{GS(F)}$ @ I_G = 1 mA	V	No Spec (o)	No Spec (o)	<2

TABLE 1

The JFET Active Filter

High input impedance of the JFET isolates the filter from the rest of the circuit. As such, all the conventional design rules apply as in bi-polar design, except for the benefits of high input impedance:

1. Reduced bandpass losses due to lower capacitance values.
2. Space saving via the smaller capacitors required.

FETs in most active filters are used as impedance transformation (isolation) devices only.

LOW-PASS FILTERS

In Fig. 1 is a typical low pass-filter including resistor R_G to provide a path for the gate dc return to ground. If voltage gain is desired, grounded source with a resistive load can be used rather than the source follower.

The voltage gain is given by:

$$Av = Av_{FET}\frac{1/j\omega C_2}{R + 1/jwC_2} = \frac{Av_{FET}}{1 + j\left(\frac{\omega}{\omega_2}\right)}$$

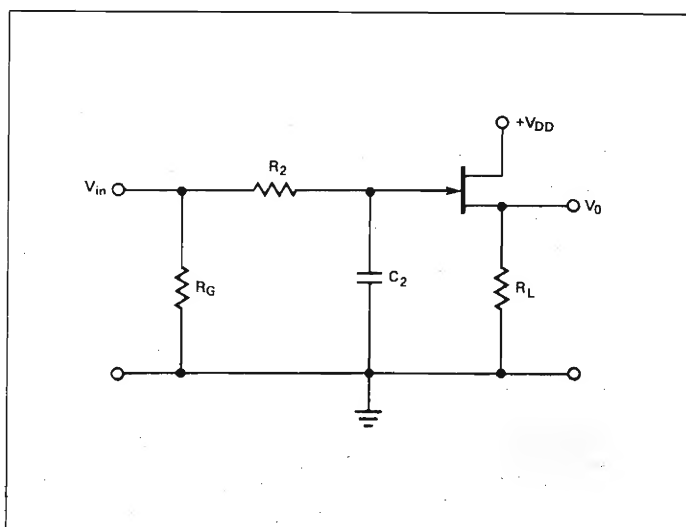



Fig. 1. Low-pass Filter (6 dB/octave)

where the 3db down angular frequency

$$\omega_2 = \frac{1}{R_2C_2} = 2\pi f_2 \quad \text{(Ref. Fig. 4)}$$

HIGH-PASS FILTERS

Fig. 2 shows a typical high pass filter.
The voltage gain is given by:

$$Av = Av_{FET}\frac{R}{R + 1/j\omega C_1} = \frac{Av_{FET}}{1 - j\left(\frac{\omega}{\omega_1}\right)}$$

where the 3db down angular frequency

$$\omega_1 = \frac{1}{R_1C_1} = 2\pi f_1 \quad \text{(Ref. Fig. 4)}$$

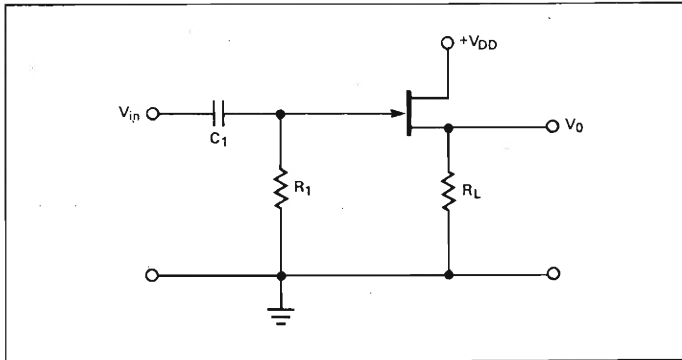



Fig. 2. High-pass Filter (6 dB/octave)

BAND PASS FILTERS

The band-pass filter is simply a combination of low-pass and high-pass filters as seen in Fig. 3. The capacitor C is limited unless a two stage FET network is used. Also R_1 should be much smaller than R_2 to minimize the coupling effects.

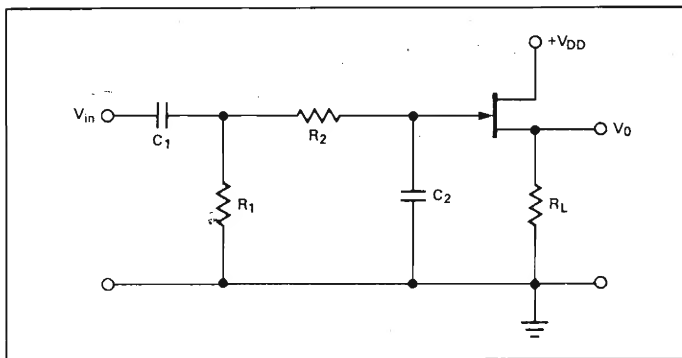



Fig. 3. Band Pass Filter (6 dB/octave)

NOTCH FILTERS

A Wein Bridge arrangement at the FET input, Fig. 5, will result in high attenuation at the design frequency. Although other methods are available, this method provides for easy tuning when gauged capacitors and resistors are used.

The notch frequency, fo, is determined by:

$$fo = \frac{1}{2\pi}\sqrt{C_1C_2R_3R_4} \quad \text{where } \frac{R_1}{R_2} = \frac{C_2}{C_1} + \frac{R_3}{R_4}$$

If ganged components and

$R_4 = 2R_3$ and $C_1 = 2C_2$; or $C_1 = C_2$, $R_3 = R_4$, and $R_1 = 2R_2$

then $fo = \frac{R_3C_1}{2\pi}$

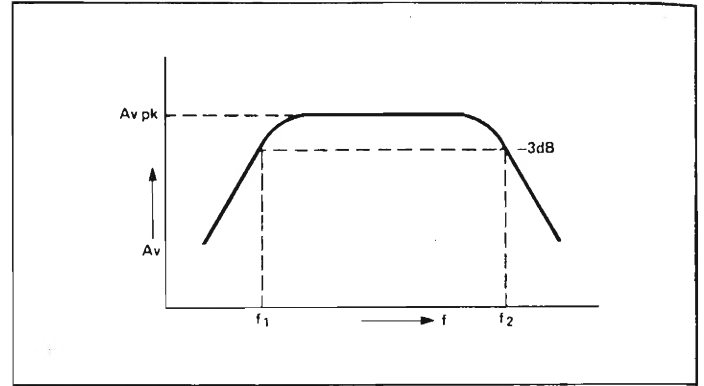



Fig. 4. Band Pass Frequency Response

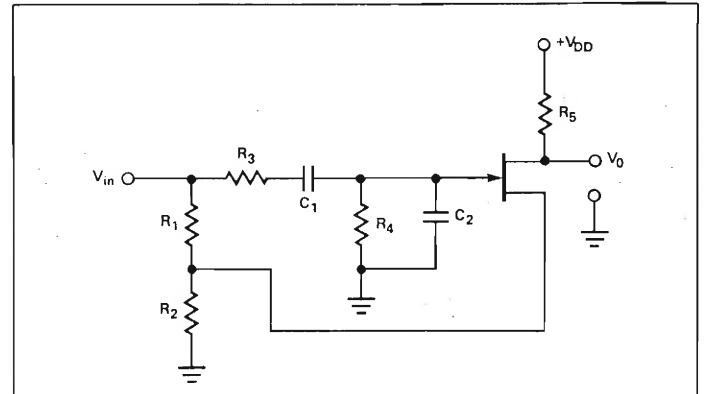



Fig. 5. Wein Bridge Notch Filter

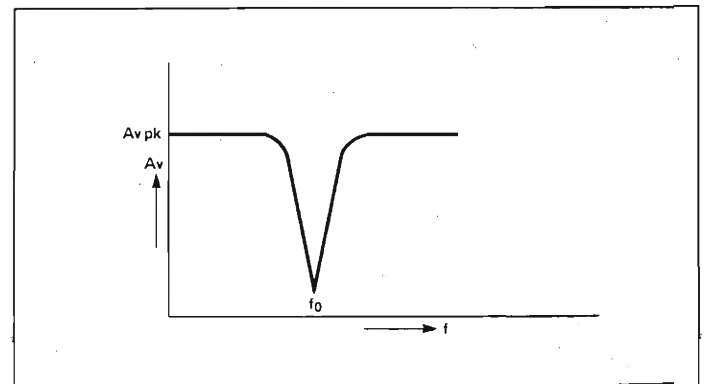



Fig. 6. Notch Filter Frequency Response

FEEDBACK FILTERS

When the filter replaces R_F in the feedback of a differential FET input operational amplifier, the frequency response of the combined arrangement will be the inverse of the passive filter.

FEEDBACK LOW-PASS FILTER

Using the high pass filter, Fig. 2, in the feedback loop

$$Av = \frac{Av_{FET}}{\dfrac{1 + Av_{FET}}{1 - j\left(\frac{\omega_2}{\omega}\right)}}$$

If $\omega >> \omega_2$ $Av = 1$
$\omega >> \omega_2$ $Av = Av_{FET}$

FEEDBACK HIGH-PASS FILTER

Using the low pass filter, Fig. 1, in the feedback loop

$$Av = \frac{Av_{FET}}{\dfrac{1 + Av_{FET}}{1 + j\left(\frac{\omega}{\omega_1}\right)}}$$

If $\omega >> \omega_1$ $Av = Av_{FET}$
$\omega >> \omega_1$ $Av = 1$

JFET Voltage Controlled Resistors

The most common usage of a FET calls for operation on the constant current portion of the characteristic for amplifiers and the fully ON or OFF state of the channel resistance for switches.

A very important aspect of channel resistance is the predictable variation with gate bias voltage. All the curves pass through the origin, and the parameter is fully bi-lateral for small excursions of V_{DS}—Figures 1 and 2.

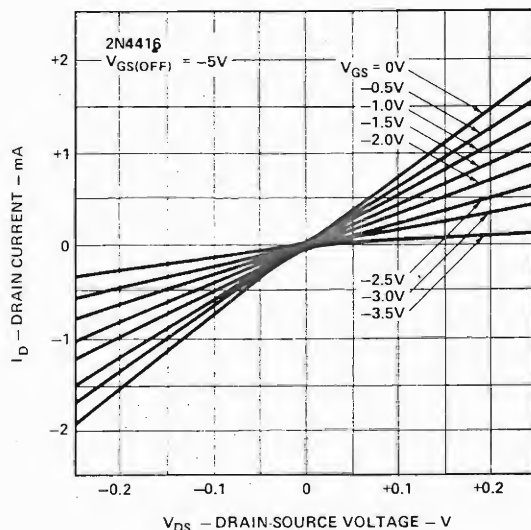



Fig. 1. Bi-lateral Characteristic

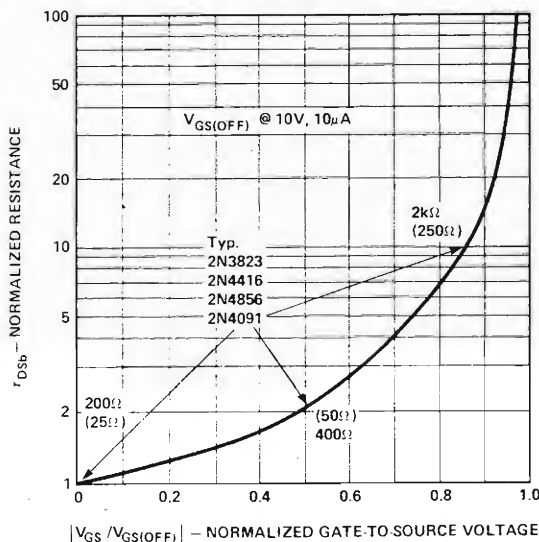



Fig. 2.

BASIC VCR EQUATIONS

Square law characteristics of the FET resemble a triode in the non-saturated region and can be expressed as:

$$\frac{I_D}{I_{DSS}} = \frac{2V_{DS}}{V_{GS\,(OFF)}}\left(\frac{V_{GS}}{V_{GS\,(OFF)}} - \frac{V_{DS}}{2V_{GS\,(OFF)}} - 1\right)$$

In terms of channel resistance, the approximation exists:

$$r_{DS} = \frac{r_{DSo}}{1 - \frac{V_{GS}}{V_{GS\,(OFF)}}}$$

In practical terms, this means that the drain characteristic is linear up to ≈ 50% $V_{GS\,(OFF)}$ and up to ≈ 25% I_D. Many applications, however, will utilize the curve > 90% $V_{GS\,(OFF)}$.

The channel resistance, a function versus temperature of the channel carrier mobility and gate-channel contact potential, changes as:

$$r_{DS_T} = r_{DS}\left(1 + 0.007\,\Delta T\right) \qquad r_{DS} @ \frac{V_{GS}}{V_{GS\,(OFF)}} \leq 0.5$$

ΔT = final temp −25°C
(r_{DS_T} increases as +T increases)

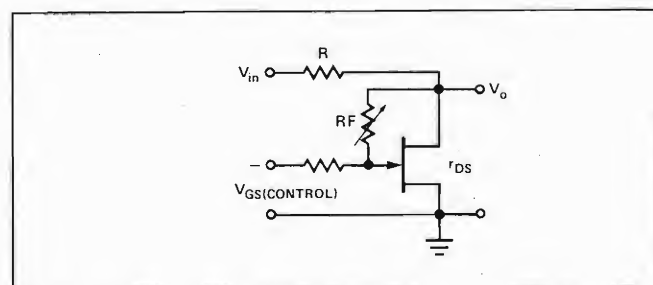



Fig. 3. Feedback-Nonsymmetrical VCR

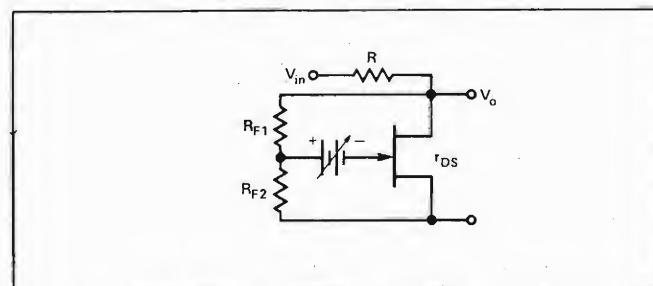



Fig. 4. Feedback Symmetrical VCR $R_{F1} = R_{F2}$

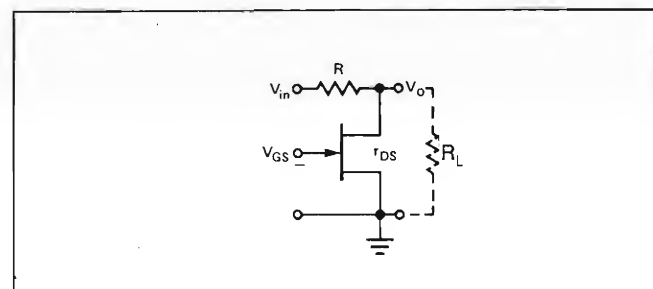



Fig. 5. Basic VCR ($R_L >> r_{DS}$)

VCR FEEDBACK

Where large V_{DS} swings are necessary affecting the linearity, feedback from the output to input through feedback Compensating for one $V_{GS(OFF)}$ device may under or over compensate another device.

BASIC VCR CALCULATIONS

The basic VCR configuration (Fig. 5) (most often used) becomes a simple voltage divider and the output voltage is

$$V_o = \frac{V_{in}\, r_{DS}}{r_{DS} + R} \quad \text{when } r_{DS} >> R \quad V_o = V_{in}$$

VCR APPLICATIONS

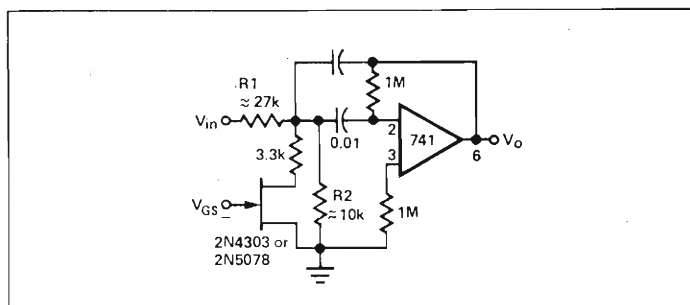



Fig. 6. Voltage tuned filter octave range with lowest frequency at JFET $V_{GS(OFF)}$ and tuned by R_2. Upper frequency controlled by R_1.

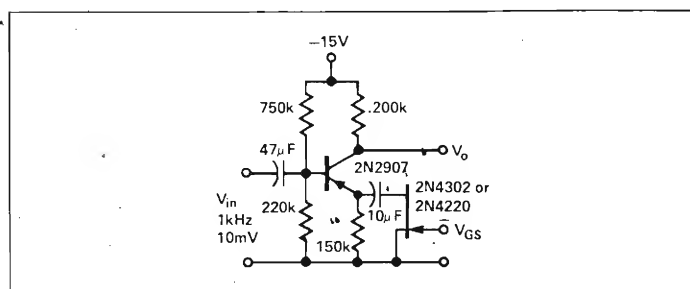



Fig. 7. Wide-dynamic-range (40 dB) AGC circuit. No gain through FET with distortion proportional to input signal signal level.

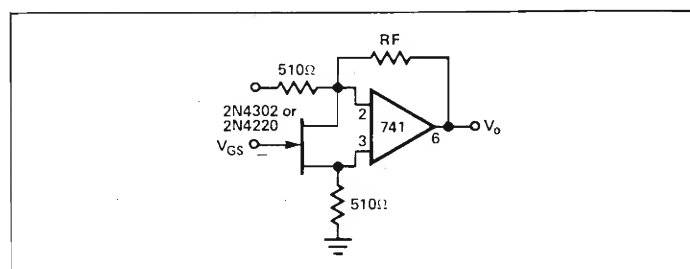



Fig. 8. Electronic gain control utilizing the low offset voltage of the 741, the JFET will have linear resistance over several decades.

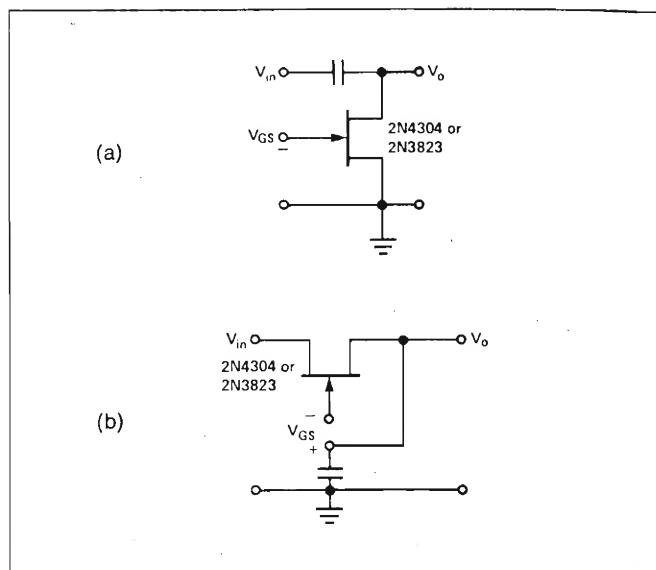



Fig. 9(a) Phase advance circuit (b) Phase retard circuit

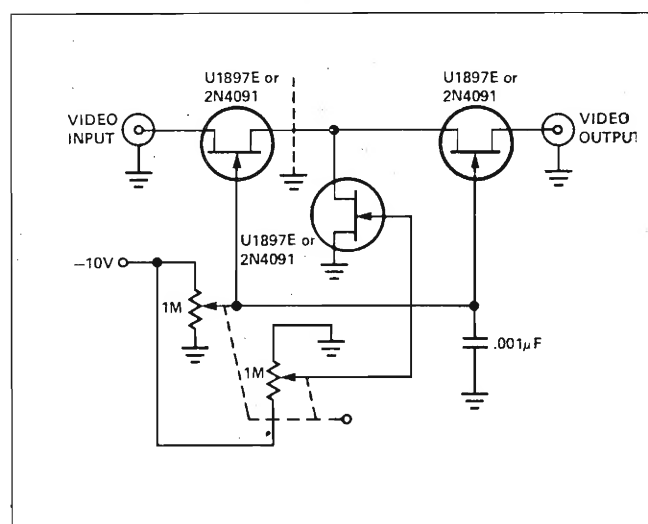
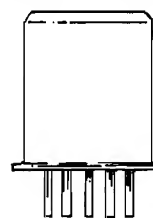



Fig. 10. Voltage controlled variable gain amplifier. The attenuator provides for optimum dynamic linear range attenuation up to 100 dB, even at f = 10.7 MHz with proper layout.

FETRON,™ solid state vacuum tube replacement

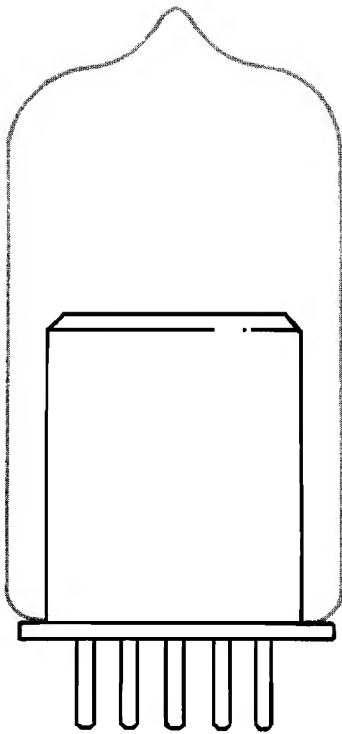
fet·ron (fet' rän) *n.* [ModE. < L. – *semiconductus* < *fetum* (? akin to *FET*, transistor), + RON (< Molaysian), orig. with reference to a solid state tube replacement introduced by Teledyne Semiconductor in 1972] **1.** An answer to improved performance and 100 year life of existing vacuum tube electronics gear **2.** A cost reduction for companies maintaining large vacuum tube systems **3.** A method of reducing the cooling requirements in buildings containing large quantities of vacuum tubes **4.** A method of reducing electric bills due to elimination of filament current **5.** [Adv.] The greatest thing since the winning of the West

FETRON

TELEDYNE SEMICONDUCTOR

Teledyne Semiconductor is a division of Teledyne, a diversified corporation with over $1.2 billion annual sales, and products ranging from insurance to steel and electronics. The Teledyne Semiconductor division was formed in 1958. Its principle purpose was to develop and market the JFET (Junction Field Effect Transistor). Many high reliability solid state components have since been developed at Teledyne Semiconductor. These components are now used throughout the electronics industry in military, industrial, and consumer applications.

The Semiconductor division now has an extensive product line that includes bipolar transistors, digital and analog integrated circuits, hybrids, and JFETs. These product technologies, principally hybrid and JFET, have been applied by Teledyne Semiconductor in the development of the FETRON, a solid state device for direct vacuum tube replacement. FETRON production uses the same proven construction methods and quality control procedures as Teledyne's ultra high reliability, military grade electronic components. As a result, the FETRON has out-performed the vacuum tube in its own socket.

Although the required technology was available in 1968, the FETRON development didn't get under way until early 1970. This was partly due to the industry trend toward complete re-design of vacuum tube equipment with all solid state devices. In development of the FETRON, Teledyne's objective was to reverse this trend and develop an economical method for retrofitting vacuum tube equipment in the field.

FETRON,[T.M.] solid state vacuum tube replacement

VACUUM TUBE TO FETRON

Prior to the development of the transistor, and particularly the high voltage JFET, electronic equipment for many applications was engineered with the vacuum tube as the principle active element. In spite of the instabilities and short life of the vacuum tube, much existing equipment, particularly telephone carrier equipment, is well designed and will last for many more years if properly serviced.

However, the servicing cycle for vacuum tube equipment is very expensive, requiring frequent adjustment and periodic tube replacement to minimize down time. As a result, most existing vacuum tube equipment is scheduled to be replaced by new all solid state equipment. But new equipment is also very expensive and requires large capitalization in most cases. Replacement of obsolete vacuum tube equipment has therefore been delayed.

As a solution to this problem, Teledyne has developed the **FETRON** for direct plug-in replacement of vacuum tubes in the field. This allows the vacuum tube equipment user to reap many of the benefits of all solid-state equipment without having to incur the expense of complete new systems. The **FETRON** provides improved equipment performance, and drastically reduces servicing costs and electric bills from the date of installation.

In high utilization equipment, such as telephone carriers, the **FETRON** can pay for itself within six months of installation. Dollar savings from the first year can then be applied toward more sensible long term equipment plans and for greater return on investment.

FETRON NOW

To date, the FETRON has been developed for replacement of pentodes and twin triodes. FETRONs are now available to replace many common tube types such as the 6AK5 and the 12AT7, described in a feature article of **Electronics Magazine**, April10, 1972. Now in development are replacement types for thyratrons, tetrodes, various high frequency tubes like the 6BA6, and power pentodes such as the 6AQ5 and the 6V6.

The FETRON is not a universal replacement for vacuum tubes, and must be configured differently for certain applications. For example, the FETRON configuration will generally be different for a pentode amplifier and an oscillator. However, the number of replacement tube types and specific applications is growing rapidly, and may one day cover virtually every tube type and application.

The FETRON is currently used mainly in telephone communications systems. Several hundred thousand are now operating in telephone carrier equipment. FETRONs in the field have replaced the 407A, 408A, and similar types. Replacement types are under development for the 403A, 404A, 415A, and 396A tubes. Other replacement types will be developed as requirements are made known by potential users.

INSIDE THE FETRON

The FETRON is composed of one or more JFETs, a protective fuse, and R/C networks for tailoring to the required circuit performance parameters. The JFETs used in the FETRON are also used in high reliability missile systems, and many other applications. These are high volume, proven devices. A tantalum fuse is used, and thick film methods are employed for the R/C networks.

Using standard hybrid circuit techniques, the FETRON elements are assembled under ultra clean conditions. The FETRON elements are then attached to a substrate, after which the substrate is soldered to the header. Using gold wires, the chips and substrate pads are attached to the posts on the header. These posts extend through the header as the socket pins.

A 3/4" nickel-plated cap is cold welded to give the standard semiconductor type hermetic seal. The cap also minimizes device temperature and allows easy plug-in to tube sockets.

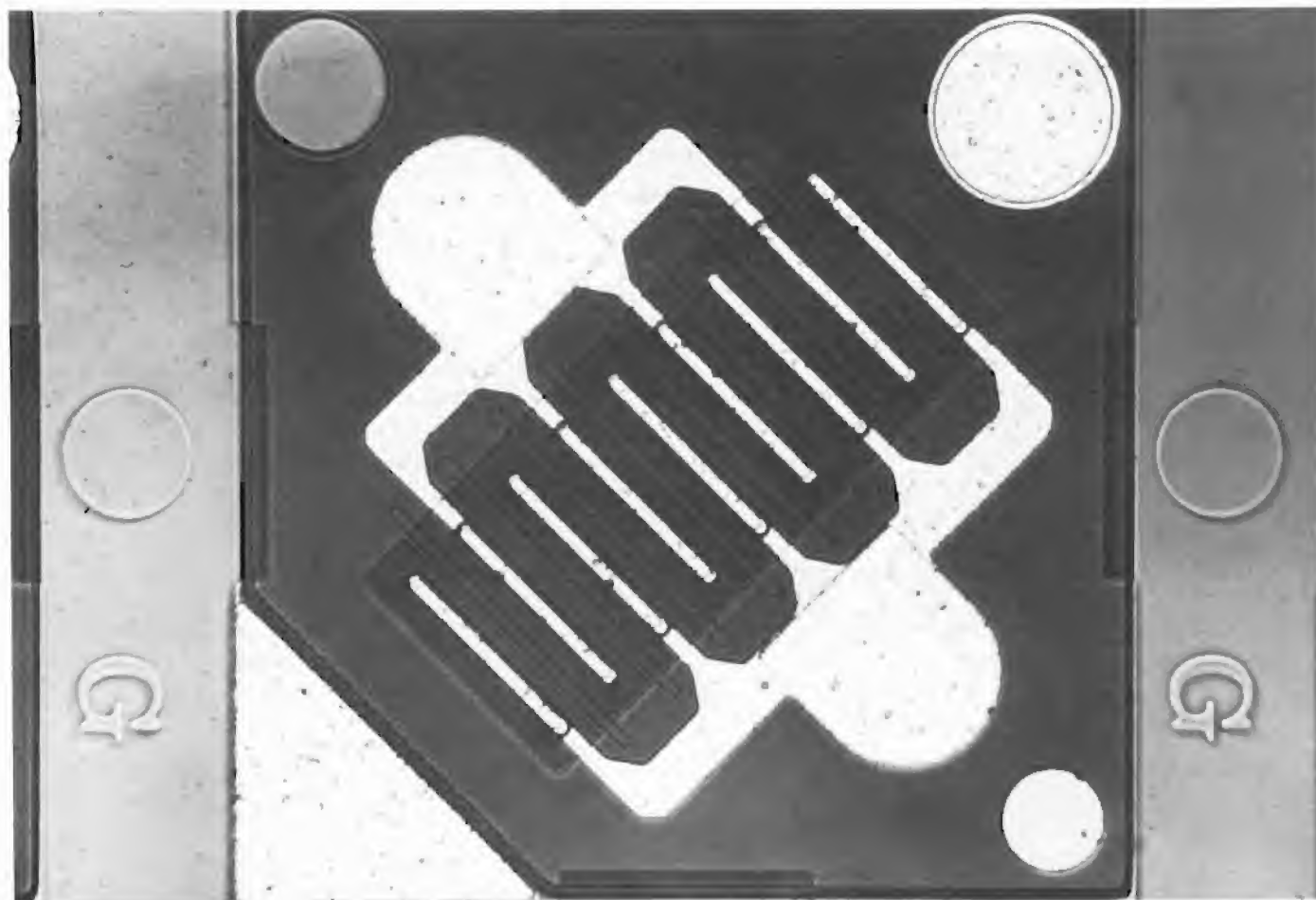



Figure 1. A Junction Field Effect Transistor (JFET). One of the JFETs used in the FETRON, and in volume production for high reliability missile systems and many other applications.

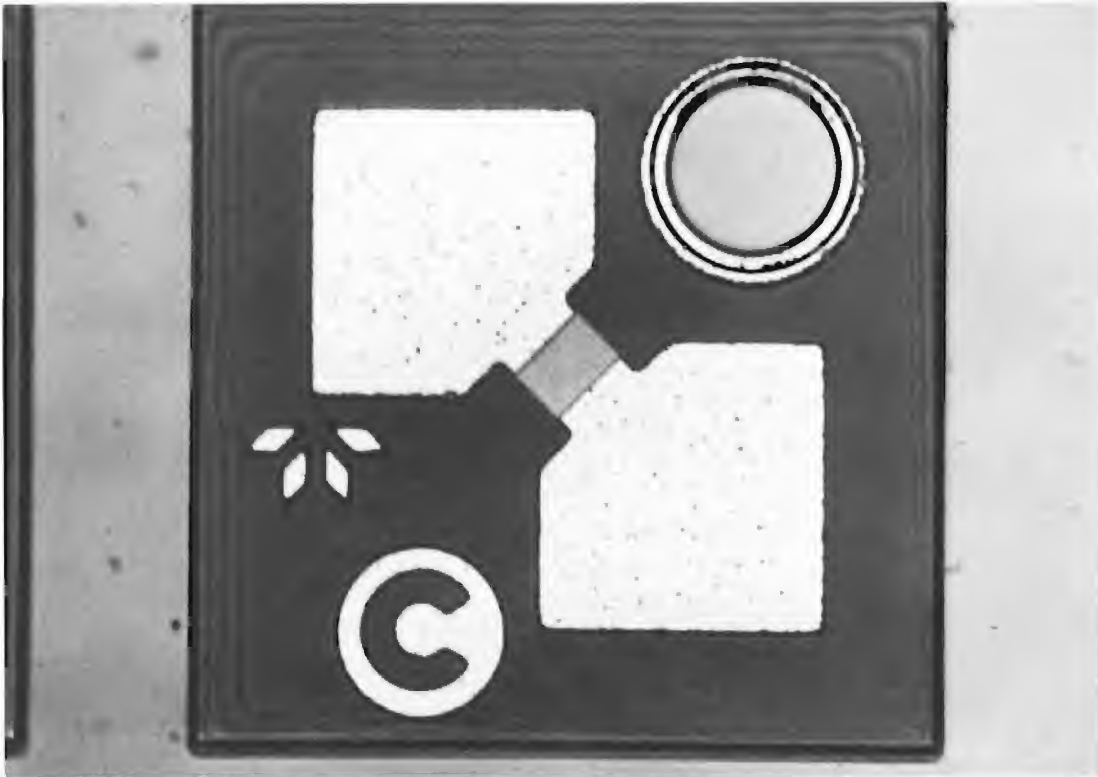



Figure 2. A Tantalum Fuse. The fusing device used for protection of other components in case of failure due to overload. The tantalum fuse, like other FETRON circuit elements, is made by well-established integrated circuit methods.

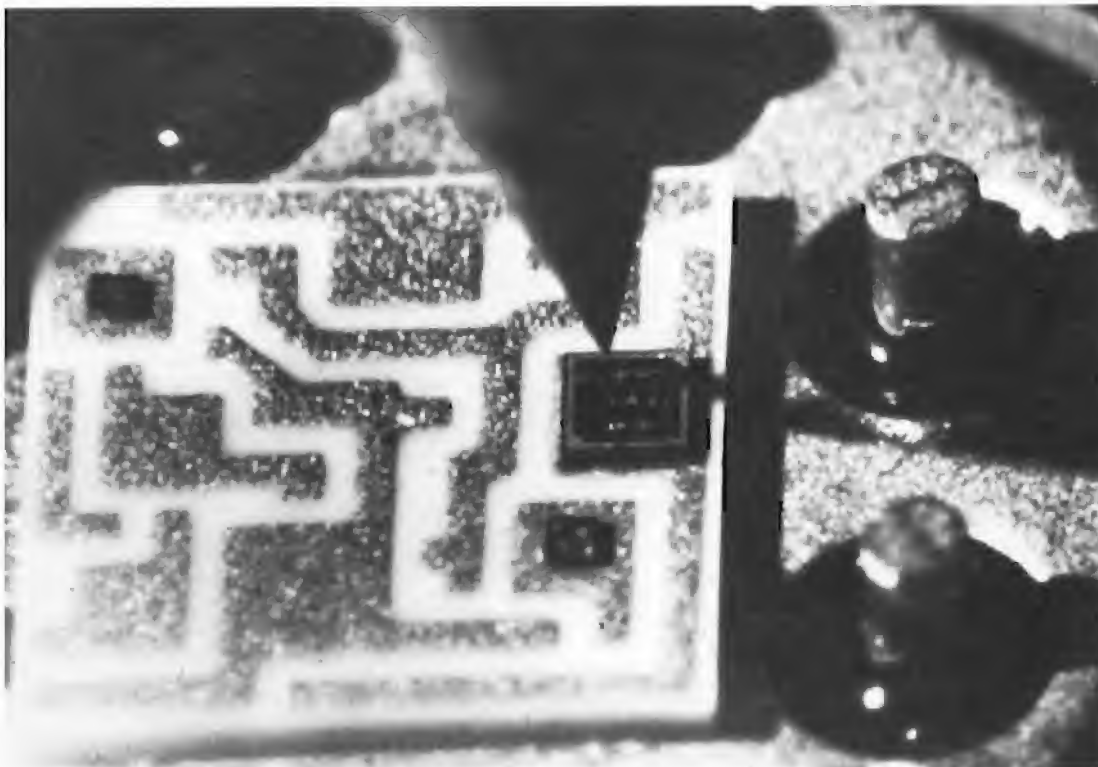



Figure 3. FETRON Circuit Assembly. FETRONs are assembled on a thick film substrate by well-established hybrid circuit methods. After bonding to the header, gold wires are connected from its pads to posts which extend through the header as pins for the vacuum tube socket.

Figure 4. FETRON Production. Methods used for assembly are the best industry quality control standards, MIL-STD-883. Assembly procedures are carefully planned and carried out under ultra-clean conditions to maximize FETRON reliability.

Figure 5. FETRON Assembly Steps. The FETRON thick film circuit is shown (1) as a clean substrate, (2) with conductive film, (3) with circuit etched, and (4) with circuit chips attached. The completed circuit is then soldered to the header and connected to the posts with gold wires. The header is then hermetically sealed with a nickel-plated cap.

HOW THE FETRON WORKS

The FETRON usually contains two JFETs connected in cascode to simulate the actual performance of a pentode or triode vacuum tube. The advantages of this configuration are:

1. The input characteristics are determined by the first device,
2. The plate voltage rating is determined by the second device, and
3. The Miller capacitance is minimized.

Since a screen grid is not needed by a FETRON, some circuits include R/C networks to simulate the equivalent circuit of the screen-plate circuit. A tantalum fuse is connected in the plate circuit to protect other circuit components in case of failure.

Using cascoded JFETs in combination with other elements, any number of different tube types can be simulated. The FETRON is most like a pentode in that the plate current is essentially independent of the plate to cathode voltage. The plate current of a triode, and its transconductance, are very much dependent on the plate to cathode voltage. The FETRON is therefore superior in principle to the triode, and usually provides improvement in circuit performance upon replacement.

However, the proper FETRON must be selected and trimmed for each application, to avoid saturation effects as determined from the load line analysis.

Because of characteristic similarity, a FETRON can very closely simulate the function of a pentode tube. The gain/phase relationships are almost identical for a FETRON and a pentode. However, there are three important circuit improvements obtained with the FETRON. These are:

1. Reduced noise by several dB, and no microphonics,
2. Higher gain which is independent of screen voltage, and;
3. Lower distortion by typically 15dB.

The pentode generates distortion by cross modulation of higher harmonics, a result of its three-halves response relationship. The FETRON, however, is close to being a perfect square law device over most of its usable range, and generates almost no harmonics above the second. The FETRON must also be tailored for pentode operating conditions, but less critically than for the triode.

In general, the choice of FETRON depends on operating voltage and power levels, frequency range and whether an oscillator or an amplifier. Teledyne has analyzed the circuits on most telephone carrier equipment and other instruments such as Hewlett Packard VTVMs. Worst case analyses have been done on the carrier equipment by Teledyne together with different telephone companies. Teledyne has also formalized simple conversion procedures in most cases. The target ground rules for specific applications are:

1. No external components.
2. No re-wiring of equipment.
3. No power supply changes.
4. Plug directly into the tube socket.

These objectives have been achieved in almost every case. They make it easy for you to reap the benefits of the FETRON.

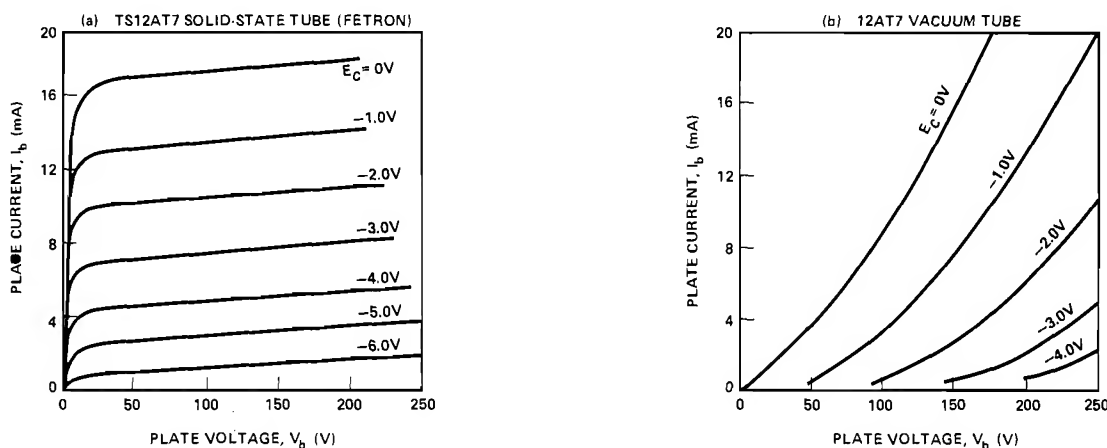



Figure 6. FETRON Compared with Vacuum Triode. The FETRON provides a plate current/voltage characteristic that is superior to the triode. Plate current in the FETRON is virtually independent of plate voltage. The plate current and transconductance of a vacuum triode is very much dependent on plate voltage. For example, with a 240 ohm load, a plate voltage change from 130V to 60V results in a plate current change from 8mA to 2.5mA. The same voltage excursion results in only μA in the FETRON.

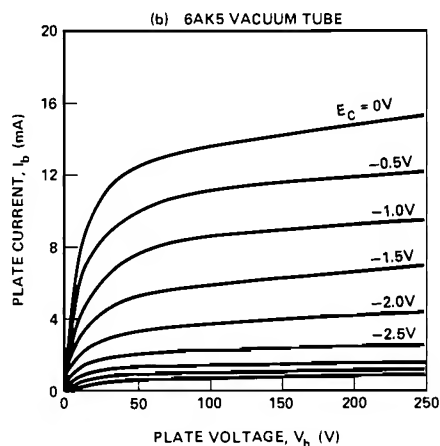
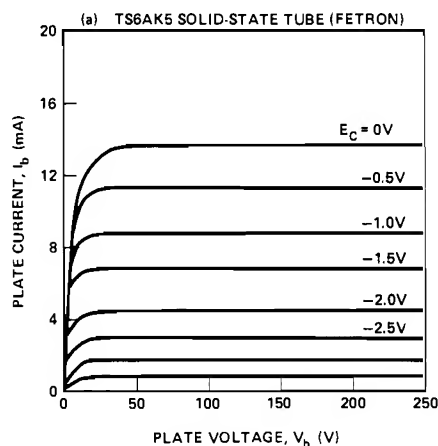



Figure 7. FETRON Compared with Vacuum Pentode. The FETRON is most like a pentode, but provides a superior plate current/voltage curve. The transconductance at the pentode is nearly independent of plate voltage, but depends on screen to plate voltage. The FETRON is independent of both. A plate voltage change from 130V to 60V causes a pentode plate current change from 10mA to 4mA. The corresponding FETRON current change is negligible.

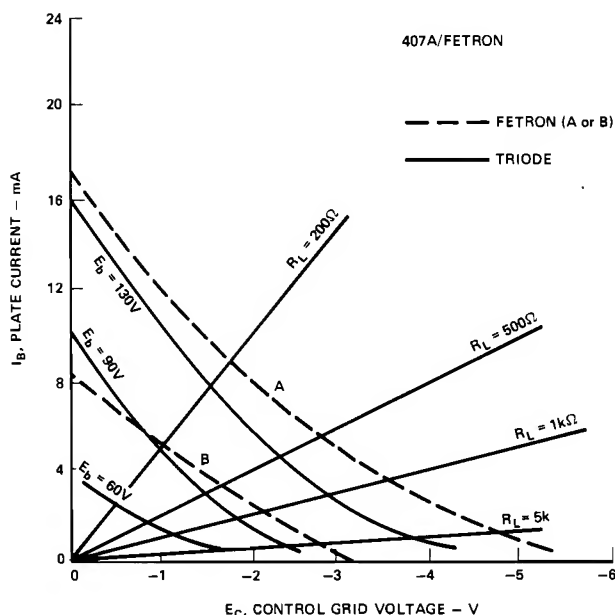



Figure 8. Transfer Characteristic, FETRON vs. Vacuum Triode. By JFET selection and trimming, any triode function can be generated. A load line analysis is conducted by Teledyne to prevent saturation when the FETRON is plugged into the tube socket. A 50kΩ load would saturate FETRON A, but not FETRON B.

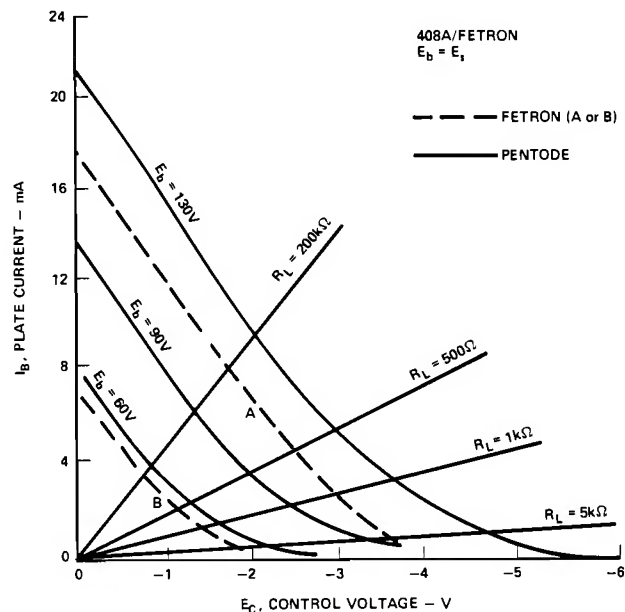



Figure 9. Transfer Characteristic, FETRON vs. Vacuum Pentode. Most vacuum pentode functions can be generated with a FETRON. The FETRON is less dependent on circuit voltage and generates less noise and microphonics.

CIRCUIT GAIN PHASE vs. FREQUENCY

PHASE IN DEGREES: 360, 240, 120, 0, 240, 120, 0
GAIN IN dB: +30, +20, +10, 0, −10, −20, −30
1K, 10K, 100K, 1 MEG, 10 MEG
f – FREQUENCY – Hz
PHASE
(VACUUM TUBE)
(FETRON)
GAIN
(FETRON)
(VACUUM TUBE)

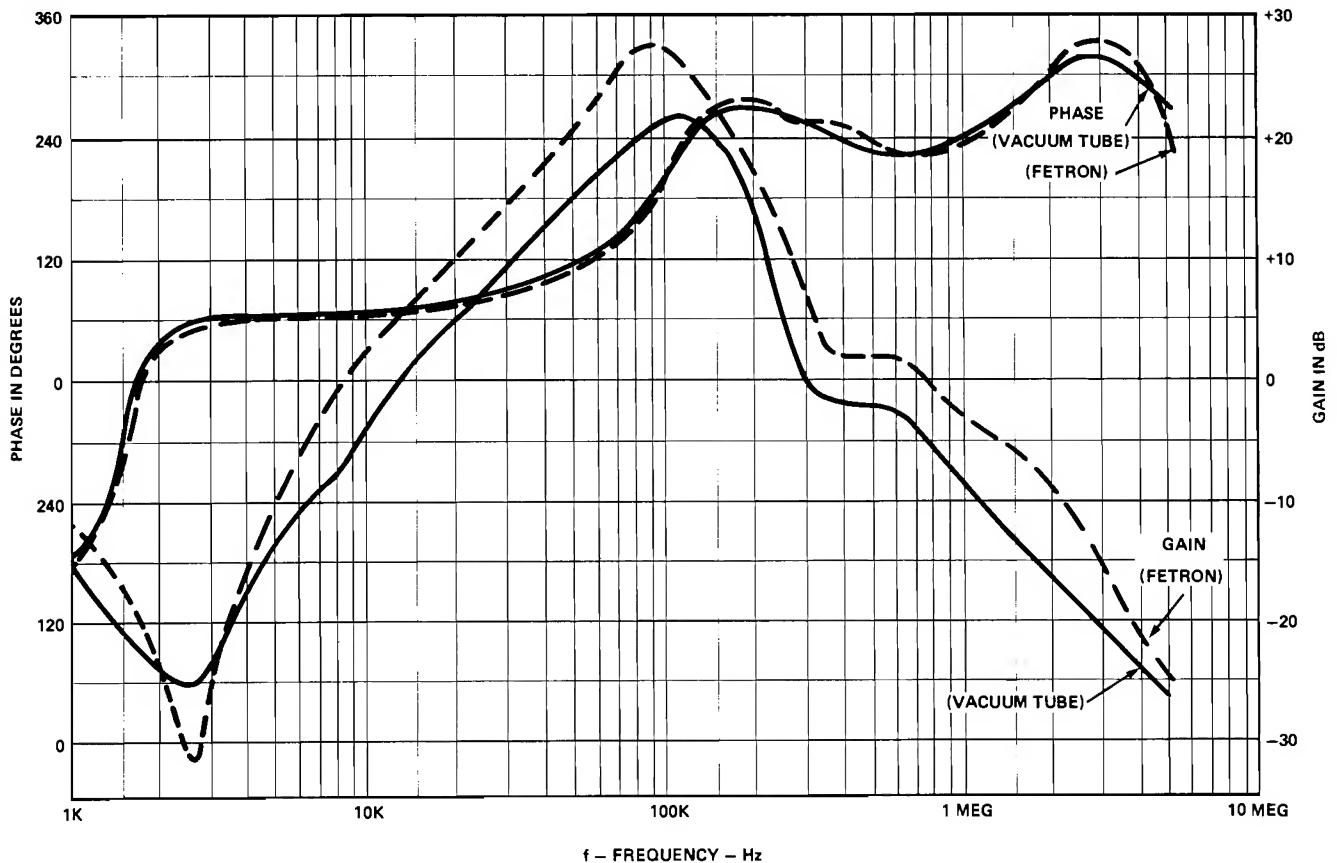



Figure 10. Frequency Response, FETRON vs. Vacuum Tube. The gain/phase curves for the FETRON and the vacuum tube are matched quite closely. No changes due to these functions are incurred. The FETRON reduces distortion due to upper harmonic by 15dB, a result of its true square law response.

FETRON BENEFITS

As a result of low initial cost of the FETRON and generous savings resulting from vacuum tube replacement, the FETRON is finding rapid and widespread acceptance. These cost savings result from the simple advantages the FETRON has over the vacuum tube. Primarily higher reliability, more stable operating characteristics, and lower power consumption. Add to this list the ease of replacement designed in by Teledyne, and the result is an irresistable opportunity for change.

Higher Equipment Reliability results from the lower operating temperature, less thermal wear on other parts, and the longer lifetime of the FETRON. Vacuum tubes have a useful life of only thousands of hours. Experience with FETRONs in the field has demonstrated a lifetime greater than one million hours, over a hundred years. The net result is extended equipment life, less down time and a savings of frayed nerves. The cost of standard industrial tube replacements alone is about $4.00 per year. Other components are estimated to be $2.00 per year for each tube, resulting from thermal wear.

Maintenance Costs are drastically reduced since FETRONs do not require periodic replacement or frequent adjustment like the vacuum tube which begins to degrade immediately after installation. As a result, there is no change in signal transmission strength or quality degradation with time. A definite improvement in quality in most cases. Estimated savings for a typical thirty tube system are:

1. Local site – 3hrs x $15/hr x 2 servicing/yr x 1/30 = $3/tube/yr.
2. Remote site – 4hrs x $25/hr x 2 servicing/yr x 1/30 = $6.67/tube/yr.

Electric Bills are much lower because FETRONs use less than half the power of vacuum tubes. Air conditioning bills are lower too, and personnel efficiency goes up along with the

Table 1. Typical FETRON Savings, $/yr/FETRON

Item of Savings	Remote/Commercial Tube Installation	Local/[illegible]Tube Installation	Your Installation
1. Reliability – 100 year FETRON	$4.00	$1.00	
2. Power Savings – on going operation	$2.40	2.40	
3. Power Savings – new addition	$4.80 (first year)	–	
4. Maintenance	$6.67	$3.00	
5. Loss of Revenue (poor service, etc.)	$1.50	$1.50	
6. Other Components – thermal wear	$2.00	$2.00	
7. Extended life of present equipment	? ? ?	? ? ?	
Total FETRON savings	$16.57+?	$9.90+?	

plant comfort index. Estimated power savings by replacement of a vacuum tube by a FETRON are:

1. Operating tube power – 1.9 W/tube x 9k hrs/yr x $.01/kW hr = $1.70/tube/yr.
2. Air conditioning, standby power, etc. – 0.9 W/tube x 9k hrs/yr x $.01/kW hr = $0.70/tube/yr.

Each equipment user has found different FETRON conversion priority and cost savings. Here are some examples of cost savings to set the wheels in motion.

- One area had maintenance problems and loud customer complaints on some repeater lines. All was quiet after conversion to FETRONs.
- A costly power panel replacement program for handling high current loads was cancelled due to the low current drain of FETRONs.
- After observing no drift in equipment calibration for a year after installation, numerous maintenance people were assigned other jobs.
- Instead of salvaging tube equipment in favor of short-lived new equipment, the older equipment lives on with FETRONs.
- After learning about FETRONs, additional batteries and diesel generator requisitions were cancelled. FETRONs eliminated the need.
- "Do I spend $20,000 for power supplies and building additions?" Just $1,600 worth of FETRONs deferred this expenditure for at least 5 years.
- Power plant additions totaling $80,000 were deferred several years. A result of –48 volt savings accrued by installation of $20,000 worth of FETRONs.
- One sizable telephone company when asked why they were so anxious for their FETRON delivery, indicated that they would be saving $5,000 a day with FETRONs.
- Several remote sites in the Midwest used a twin DC to DC converter (two in case one failed), working off the –48V system. They were able to avoid increasing the –48V drain since filament current was eliminated with FETRONs. As a result, a +130 supply and standby batteries were pulled out, making room for new carrier systems.
- One group installed FETRONs in equipment scheduled for removal within two years, still realizing a substantial savings with FETRONs. Unlike vacuum tubes that wear out, the FETRONs will be used elsewhere when the equipment is turned down.
- All groups like the advantage of immediate write-off maintenance money, rather than having to capitalize new equipment.

  "We can now meet the tighter standards imposed on us without huge expenditures."

These profitable success stories are a result of careful engineering, and cooperative effort to solve the problems involved. The solution to these individual problems has resulted in a catalog of FETRON conversion kits available from Teledyne Semiconductor.

FETRON KITS

Numerous systems have been converted to FETRONs throughout the North American Continent. Other systems are in a field trial stage. Still others are in the prototype stage. As a result, a number of FETRON conversion kits are available in various phases of development.

Conversion of these systems available immediately:

N1 Repeater (–130V or tandem)
N1 Terminals (save > 200W)
ON Carrier (stable, low W)
O Carrier (stable, low W)
O Repeater (low noise)
HP 400 VTVM (low noise)
E2, E3 Repeaters (simple conversion)
V3 Voice Amplifiers (simple conversion)
MF Receivers (all solid state)
Lenkurt 45A Carrier (no drift)
43A1 Teletype (all solid state)

These systems are in field trials, available June, 1973:

Lenkurt 45BN Cable Carrier
Lenkurt 45BX Radio Carrier
ANI Identifier
Lynch B510 Carrier

These systems are in the prototype stage, some available data:

ON Junction
TD2 70MHz IF
Lenkurt 74, 70MHz IF
Lenkurt 4564 Repeater

Begin your investigations with the systems we have now. Teledyne stands ready to work with you on systems in development, or new systems to suit individual needs.

MAKE FETRONS PAY

If you have vacuum tube equipment in your facility, FETRONs will save money for you. The following is a suggested approach to determine how. It has been compiled from experience by applications of FETRONs at Teledyne.

1. Survey your equipment for the number and types of tubes, and types of equipment.
2. Consider setting up trial locations for field tests for the most pressing needs. Evaluate the results.
3. Teledyne will support your investigation with applications assistance. Take an in-depth look at the savings achievable with the FETRON.
4. Let Teledyne know your needs. They have experience where it counts and are anxious to help.

For immediate information or assistance, contact:

Teledyne Semiconductor
1300 Terra Bella Ave.
Mountain View, California 94043
Phone: 415/968-9241

FETRON®
Solid State Vacuum Tube Replacement

TS6AK5 Series

Features

- ZERO WARM-UP
- NO MICROPHONICS
- REDUCED HEAT RADIATION
- MECHANICALLY RUGGED
- TRUE CUTOFF WHEN USED AS SWITCH
- NO SCREEN GRID POWER
- SEMICONDUCTOR RELIABILITY
- LOW NOISE/DISTORTION
- DIRECT REPLACEMENT
- NO HEATER OR SCREEN GRID POWER
- NO TRANSCONDUCTANCE
- DEGRADATION WITH TIME

Connection Diagram

N/C
N/C
P
4
3
5
SOLID
STATE
ARRAY
K_{I_S} 2
6 N/C
1
7
G_1
K_{I_S}

Description

The TS6AK5 Series is a 7-pin miniature pentode in a metal hermetic sealed package. It is designed for direct replacement of conventional glass vacuum tubes where greater reliability, stability, and performance are desired. It can be used in RF or IF amplifiers/receivers, and in high-frequency wide-band applications up to 200 megahertz. It also excels in audio-frequency application exhibiting no microphonic noise and negligible 1/f noise. Low power consumption is ideal for mobile equipment tube replacement. Three types are available to meet differing applications.

Physical Dimensions

.556/.544 DIA
.789/.771
.046 MAX
.260/.240
7 LEADS
.042/.038 DIA
.665/.655 DIA
.380/.370 DIA
45°

Maximum Ratings

Plate Voltage	180 V
Grid – No. 2 (Screen-Grid) Voltage	N/C
Grid – No. 1 (Control-Grid) Voltage, Positive-bias value	0 V
Plate Dissipation	3.0 W
Screen Grid Dissipation	0 (N/C)
Plate Current	30 mA
Heater-Cathode Voltage	N/C
Operating Temperature Range	–25°C to +125°C

SIMILAR TS6AK5 FAMILY REPLACEMENT TYPES

6AG5, 6AK5W, 403A, 403B. 408A, 5591, 5654, 6028, 6096, 6186, 6968, 7543.

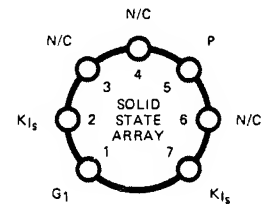
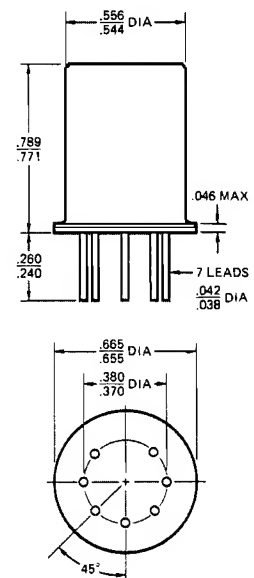
Foreign:

6F32, 12F31, DP61, E95F, EF90F, EF94, EF95, EF96, EF905, HF93, HF94, PM05, M8100, M8180.

Other Available FETRONS

2D21, 6AL5, 6AM6, 6AU6, 6BC5, 6BH6, 6CB6, 6CE5, 6J6, 12AT7, 12AX7, 404A, 407A, 415A, 5590, 5670, 5847, 6688, 7721, E180F.

TELEDYNE SEMICONDUCTOR

FETRON is a registered trademark of Teledyne Semiconductor.

General Characteristics

Heater Voltage	N/C (Open)
Heater Current	N/C
Grid No. 1 to Plate Capacitance	0.02 $\mu\mu$F
Grid No. 1 to Cathode Capacitance	4.0 $\mu\mu$F
Grid No. 2 and Grid No. 3 Capacitance	N/C

Recommended Applications by Type

TS6AK5/A1 – This FETRON is designed for general purpose applications at operating frequencies up to 30 MHz. Typical applications include telephone type carriers, FM IF strips operating at 10.7 MHz, Hi-Frequency receivers through the 10 meter band, and DC applications such as analog computers. It is not recommended for use an an FM Limiter.

TS6AK5/A2 – This FETRON should be used in those 6AK5 circuits heavily biased for low plate current operation and having high plate load resistances, typically above 5000 ohms.

TS6AK5/A3 – This FETRON is designed for VHF operation between 30 and 200 MHz. It duplicates 6AK5 vacuum type operating dynamic characteristics up to about 300 MHz. When use in RF Tuners is anticipated, the receiver AGC range should be compared with the TS6AK5/A3 cutoff characteristics to ensure proper operation.

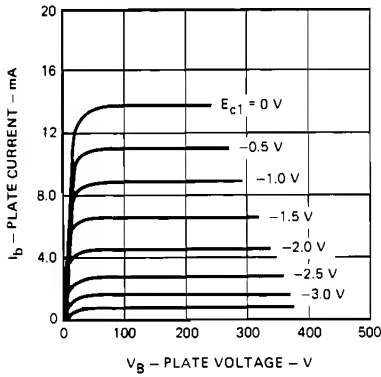
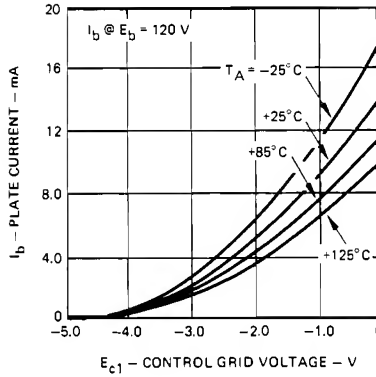
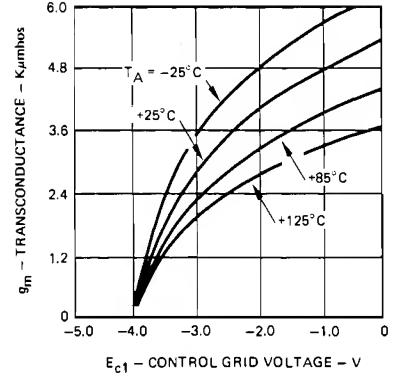
Operating Conditions and Characteristics (At 25°C unless otherwise specified)

Characteristic	Condition	TS6AK5/A1			TS6AK5/A2			TS6AK5/A3			Units
		General Purpose			Low Current			Hi-Frequency			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Plate Supply Voltage			130	180		130	180		130	180	V
Grid No. 2 Supply Voltage			N/C			N/C			N/C		
Cathode Bias Resistor			200			200			200		Ω
Plate Resistance		0.5	5.0		0.5	5.0		0.5	5.0		MΩ
Transconductance @ 1 kHz	R_K = 200 Ω C_K = 4.0 μF	3500	4500	7500	2000	3500	7500	2800	3400	6000	μMHOS
Grid No. 1 Voltage	I_D = 10 μA		−5.0	−8.5		−2.5	−6.0	−3.5		−8.5	V
Plate Current	R_K = 200 Ω	4.0	7.0	10	1.5	3.0	4.5	2.8	4.0	8.0	mA
Grid No. 2 Current			N/A			N/A			N/A		
Useful Frequency Limit			30			30			100	200	MHz
Grid No. 1 Current	E_{c1} = −12 V		0.01	0.1		0.01	0.1		0.01	0.1	μA
Case Operating Temperature	P_p = 2.0 W		67			67			67		°C
Noise Figure	100 MHz									2.0	dB

NOTE: In series filament circuits, all tubes must be replaced by solid state replacements or appropriate resistor connected externally between pins 3 and 4. Some applications may require modified TS6AK5. Consult Teledyne Semiconductor for application information.

TS6AK5/A1

Typical Characteristics

PLATE CHARACTERISTIC

TRANSFER CHARACTERISTIC

TRANSCONDUCTANCE CHARACTERISTIC

BY-PASSED PLATE CHARACTERISTIC

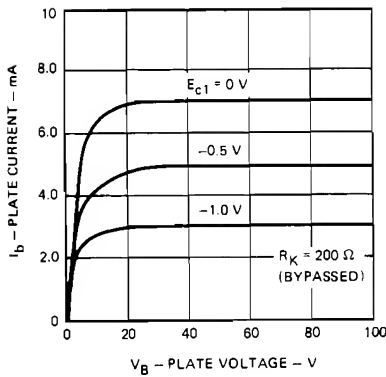
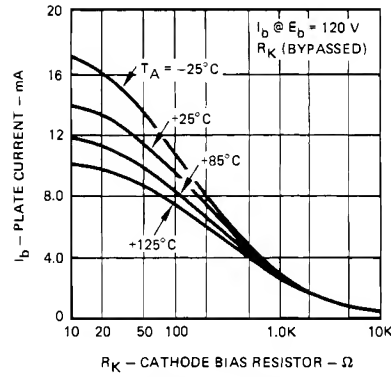
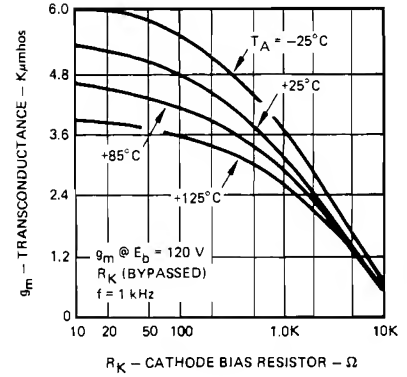



PLATE CURRENT VS. CATHODE BIAS

TRANSCONDUCTANCE VS. CATHODE BIAS

TS6AK5/A2 TS6AK5/A3

Typical Characteristics

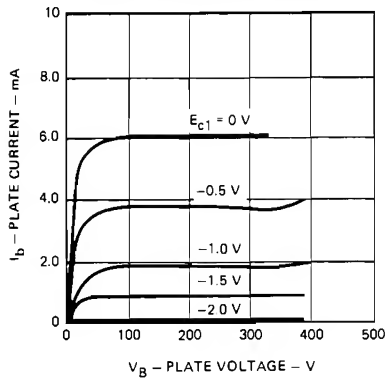
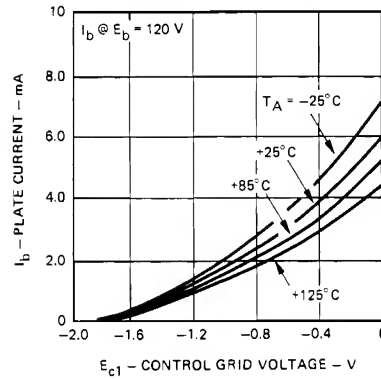
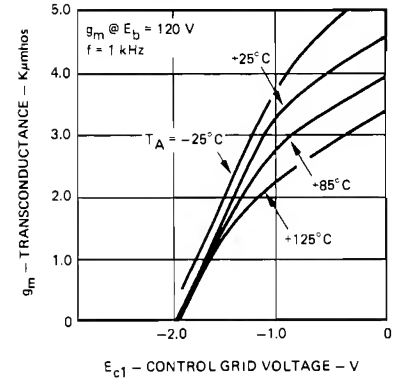



PLATE CHARACTERISTIC

TRANSFER CHARACTERISTIC

TRANSCONDUCTANCE CHARACTERISTIC

BY-PASSED PLATE CHARACTERISTIC

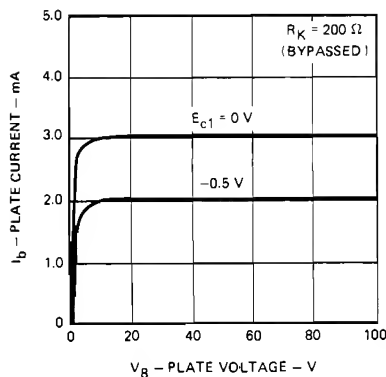
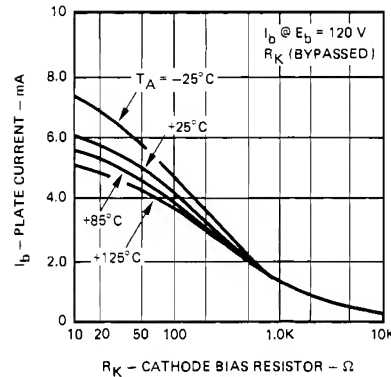
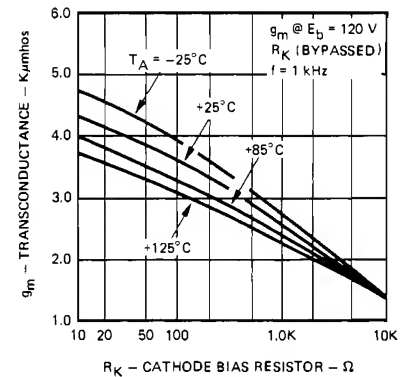
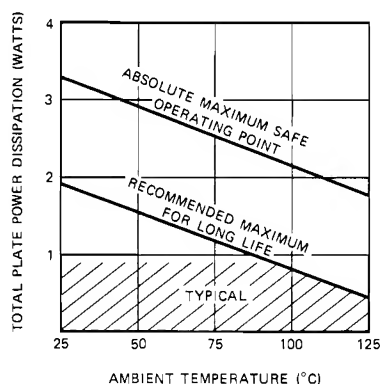



PLATE CURRENT VS. CATHODE BIAS

TRANSCONDUCTANCE VS. CATHODE BIAS

STEP 1

Determine the plate power dissipation from the circuit of the vacuum tube to be replaced. Use the highest ambient temperature in which the FETRON is expected to operate. Check the chart to ensure that the maximum safe operating point is not exceeded. The recommended maximum shown on the chart is established for a median lifetime of 300,000 hours (34 years).

STEP 2

In series filament circuits, short circuit the filament socket pins (Nos. 3 and 4) and place a 39 Ω, 2 W resistor in series at a convenient location in the filament string. (Special FETRONS with pins 3 and 4 internally short-circuited can be supplied. Consult factory representative).

STEP 3

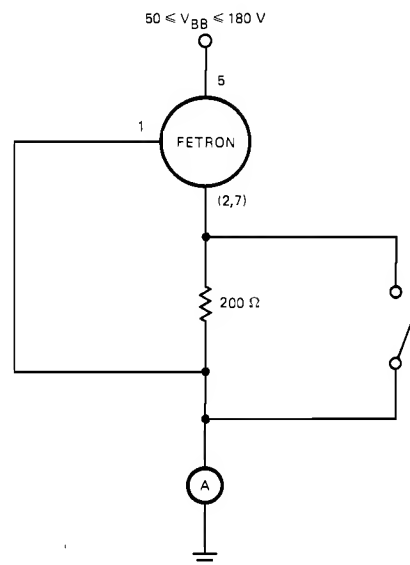
Check the plate load resistance. If it exceeds 5000Ω select Fetron type TS6AK5/A2.

STEP 4

Check the grid circuit AGC and cathode bias resistor. The FETRON should not be used with positive grid-to-cathode bias or in class C operation wherein grid-to-cathode peak positive bias exceeds +1.0 volts. If AGC bias voltage developed in the receiver exceeds −5.0 volts, it is recommended that AGC bias be divided down to −5.0 volts maximum.

How to Test FETRONS

The recommended equipment for testing FETRONS is a vacuum tube or semiconductor curve tracer, such as the Tektronix Model 575. Some mutual-transconductance type tube testers, such as the Hickok Model 539C or 752A, may be used with caution for limited testing but **DO NOT TEST FOR SHORTS OR GASSY TUBES. DO NOT TEST A FETRON WITH AN EMISSION TYPE TUBE TESTER UNDER ANY CIRCUMSTANCES.** Factory warranties are void for all FETRONS tested in such manner.

If a suitable test method is not available, the simple circuit below may be used.

(A) Open the switch. Read cathode (plate) current, I_O. Interpret grid voltage from the formula: $V_G = I_O \cdot 200$.

(B) Close the switch and read cathode (plate) current, I_C.

(C) Interpret transconductance from the formula:

$$g_m = \frac{\Delta I_P}{\Delta V_G} \simeq \frac{I_C - I_O}{V_G} \simeq .005\left(\frac{I_C}{I_O} - 1\right), \text{ m Mhos}$$

TELEDYNE SEMICONDUCTOR

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MARCH 1974

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TELEDYNE SEMICONDUCTOR

TS6AM6*

*Note: Patent Pending

TS6AM6*
Solid State Vacuum Tube Replacement

Features

- ZERO WARM-UP
- NO MICROPHONICS
- REDUCED HEAT RADIATION
- MECHANICALLY RUGGED
- TRUE CUTOFF WHEN USED AS SWITCH
- 500 MHz PERFORMANCE
- NO SCREEN GRID POWER
- SEMICONDUCTOR RELIABILITY
- LOW NOISE/DISTORTION
- DIRECT REPLACEMENT
- NO HEATER POWER
- INTERNALLY RF SHIELDED
- NO TRANSCONDUCTANCE DEGRADATION WITH TIME

Description

The TS6AM6 is a 7-pin miniature pentode in a metal hermetic sealed package. It is designed for direct replacement of the conventional glass vacuum tubes where greater reliability, stability, and performance are desired. Application is primarily in Rf or If amplifiers/receivers especially in high-frequency wide-band applications up to 500 megahertz. It also excels in audio-frequency application exhibiting no microphonic noise and negligible 1/f noise. Low power consumption is ideal for mobile equipment tube replacement.

Maximum Ratings

Plate Voltage	300 Volts
Grid – No. 2 (Screen-Grid) Voltage	N/C
Grid – No. 1 (Control-Grid) Voltage, Positive-bias value	0 Volts
Plate Dissipation	2.5 Watts
Screen Grid Dissipation	0 (N/C)
Heater-Cathode Voltage	N/C
Operating Temperature Range	–25°C to +125°C

SIMILAR TS6AM6 FAMILY REPLACEMENT TYPES

6AK5W, 5654, 6AG5, 6BC5, 6AU6, 12AU6, 7543, 6BH6, 6DT6-A, 12AW6, 3AU6, 3BC5, 3DT6, 4AU6, 4BC5, 408A, 403B, 415A, 6DC6, 403A, 6CE5, 1220, 5591, 6096, 6968, 6136, 6186, 6265, 6661, 7693, 6028.

Foreign:
6F32, DP61, E95F, EF905, EF96, EF94, 12F31, HF93, HF94, EF90F, EF95, M8100, M8180, PM05.

Physical Dimensions

Connection Diagram

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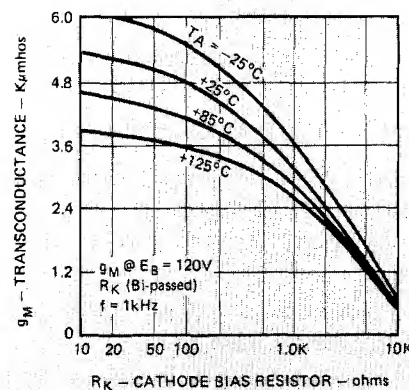
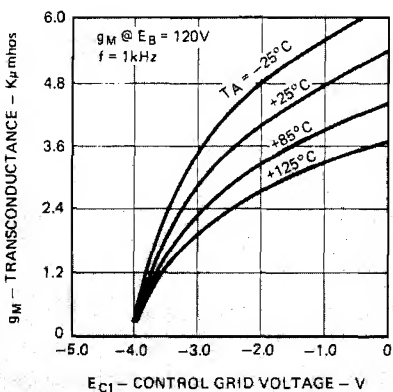
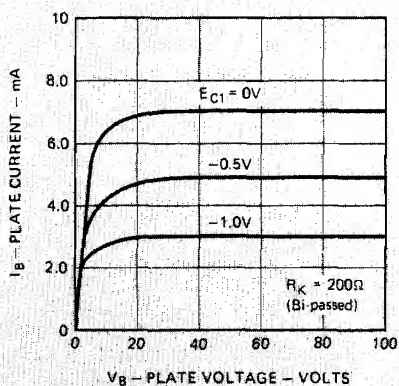
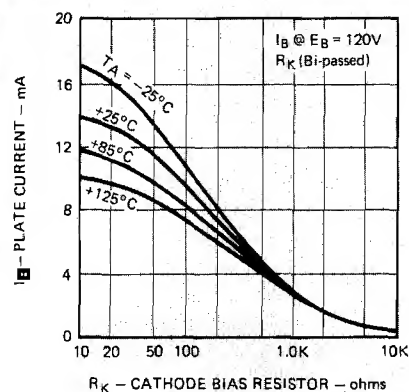
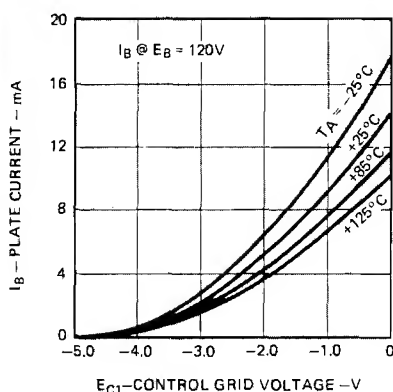
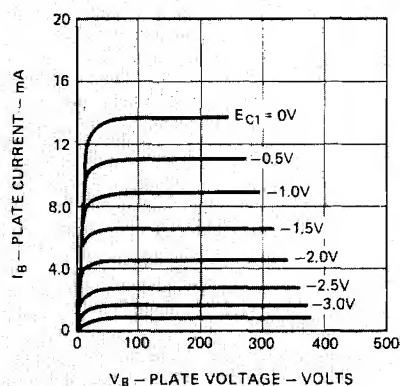
March 1973

1973/Printed in U.S.A.

General Characteristics (Stated in conventional tube terminology)

Heater Voltage	N/C (Open)
Heater Current	N/C
Grid No. 1 to Plate Capacitance	0.02μF
Grid No. 1 to Cathode Capacitance	8.0μF
Grid No. 2 and Grid No. 3 Capacitance	N/C

Operating Conditions and Characteristics (At 25°C unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Units
Plate Supply Voltage	E_b		250	300	V
Grid No. 2 Supply Voltage	E_{C2}		N/C		
Grid No. 1 Voltage	E_{C1}		−2		V
Plate Resistance	r_p	0.5	3.0		MΩ
Transconductance	gm	4000	6500	9000	μmhos
Grid No. 1 Voltage for 10μA Plate Current	E_{C1}		− 6.0	−10.0	V
Plate Current	I_b	4.0	10	13	mA
Grid No. 2 Current	I_{C2}		N/C		
Amplification Factor	μ	2000	19500		
Grid Current	I_{C1}		0.5	100	nA

Average Plate Characteristics

NOTE: In series filament circuits, all tubes must be replaced by solid state replacements or appropriate resistor connected externally between pins 3 and 4. Some applications may require modified TS6AM6. Consult Teledyne Semiconductor for application information.

TELEDYNE SEMICONDUCTOR

TS6CB6A*

*Note: Patent Pending

TS6CB6A*

Solid State Vacuum Tube Replacement

Features

- ZERO WARM-UP
- NO MICROPHONICS
- REDUCED HEAT RADIATION
- MECHANICALLY RUGGED
- TRUE CUTOFF WHEN USED AS SWITCH
- NO SCREEN GRID POWER
- SEMICONDUCTOR RELIABILITY
- LOW NOISE/DISTORTION
- DIRECT REPLACEMENT
- NO HEATER POWER
- INTERNALLY RF SHIELDED
- NO TRANSCONDUCTANCE DEGRADATION WITH TIME

Description

The TS6CB6A is a 7-pin miniature pentode in a metal hermetic sealed package. It is designed for direct replacement of the conventional glass vacuum tubes where greater reliability, stability, and performance are desired. Application is primarily in Rf or If amplifiers/receivers especially in high-frequency wide-band applications up to 175 megahertz. It also excels in audio-frequency application exhibiting no microphonic noise and negligible 1/f noise. Low power consumption is ideal for mobile equipment tube replacement.

Maximum Ratings

Parameter	Rating
Plate Voltage	300 Volts
Grid — No. 2 (Screen-Grid) Voltage	N/C
Grid — No. 1 (Control-Grid) Voltage, Positive-bias value	0 Volts
Plate Dissipation	2.5 Watts
Screen Grid Dissipation	0 (N/C)
Heater-Cathode Voltage	N/C
Operating Temperature Range	−25°C to +125°C

SIMILAR TS6CB6A FAMILY REPLACEMENT TYPES

6AK5W, 5654, 6AG5, 6BC5, 6AU6, 12AU6, 7543, 6BH6, 6DT6-A, 12AW6, 3AU6, 3BC5, 3DT6, 4AU6, 4BC5, 408A, 403B, 415A, 6DC6, 403A, 6CE5, 1220, 5591, 6096, 6968, 6136, 6186, 6265, 6661, 7693, 6028, 6AM6.

Foreign:
6F32, DP61, E95F, EF905, EF96, EF94, 12F31, HF93, HF94, EF90F, EF95, M8100, M8180, PM05.

Physical Dimensions

.556/.544 DIA
.789/.771
.046 MAX
.260/.240
7 LEADS
.042/.038 DIA
.665/.655 DIA
.380/.370 DIA
45°

Connection Diagram

N/C 4
N/C 3
P 5
K_1, G_3 2
SOLID STATE ARRAY
6 N/C
G_1 1
7 N/C

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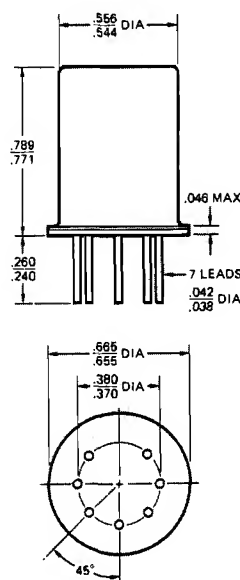
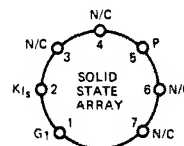
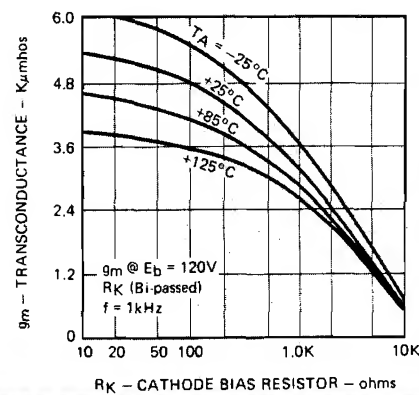
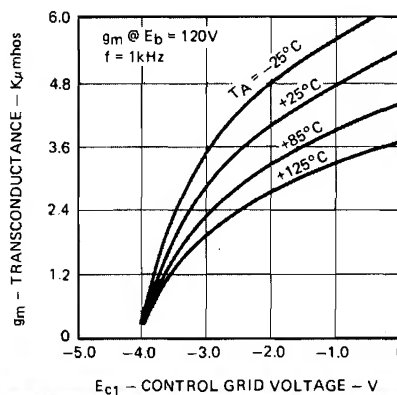
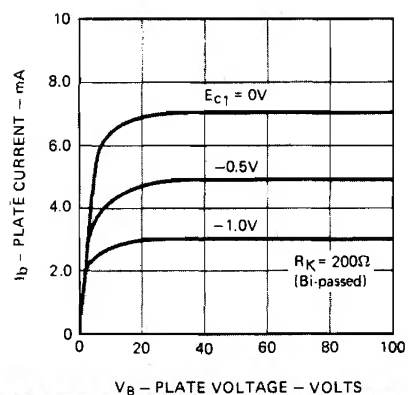
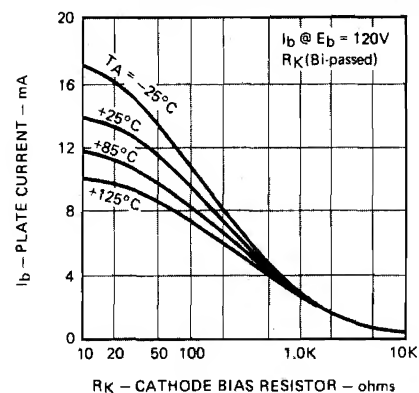
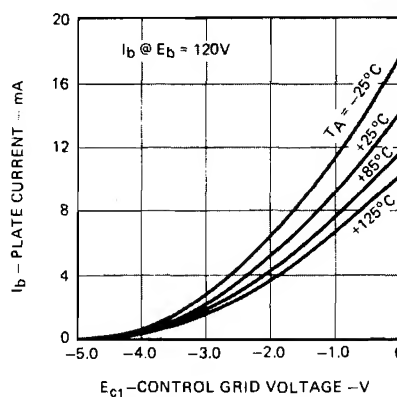
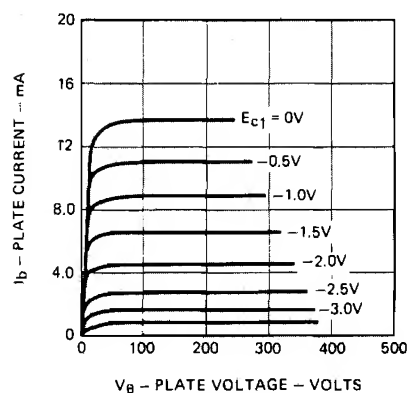

General Characteristics (Stated in conventional tube terminology)

Heater Voltage	N/C
Heater Current	N/C (Open)
Grid No. 1 to Plate Capacitance	0.02μμF
Grid No. 1 to Cathode Capacitance	8.0μμF
Grid No. 2 and Grid No. 3 Capacitance	N/C

Operating Conditions and Characteristics (At 25°C unless otherwise specified)

Characteristic	Symbol	Min.	Typ.	Max.	Units
Plate Supply Voltage	Eb		125	300	V
Grid No. 2 Supply Voltage	Ec_2			N/C	
Grid No. 1 Voltage	Ec_1		–3		V
Plate Resistance	rp	0.5	3.0		MΩ
Transconductance	gm	4000	7000	9000	μmhos
Grid No. 1 Voltage for 10μA Plate Current	Ec_1		–6.0	–10.0	V
Plate Current	Ib	4.0	10	13	mA
Grid No. 2 Current	Ic_2		N/C		
Amplification Factor	μ	2000	21000		
Grid Current	Ic_1		0.5	100	nA

Average Plate Characteristics

NOTE: In series filament circuits, all tubes must be replaced by solid state replacements or appropriate resistor connected externally between pins 3 and 4. Some applications may require modified TS6CB6A. Consult Teledyne Semiconductor for application information.

TELEDYNE SEMICONDUCTOR

TS12AT7*

*NOTE: Patent Pending.

TS12AT7*
Solid State Vacuum Tube Replacement

Features

- ZERO WARM-UP
- NO MICROPHONICS
- REDUCED HEAT RADIATION
- MECHANICALLY RUGGED
- TRUE CUTOFF WHEN USED AS SWITCH
- NO SCREEN GRID POWER
- SEMICONDUCTOR RELIABILITY
- LOW NOISE/DISTORTION
- DIRECT REPLACEMENT
- NO HEATER POWER
- INTERNALLY RF SHIELDED
- NO TRANSCONDUCTANCE DEGRADATION WITH TIME

Description

The TS12AT7 is a 9-pin miniature double triode in a metal hermetic sealed package. It is designed for direct replacement of the conventional glass vacuum tubes where greater reliability, stability, and performance are desired. It is used as push-pull cathode-drive amplifier or frequency converter in the FM range, multivibrators or oscillators in industrial control devices, phase inverters, clamp circuit, relay drivers, and other diversified applications. The low power consumption makes it ideal for mobile equipment tube replacement.

Maximum Ratings

Parameter	Value
Plate Voltage	250 Volts
Grid Voltage, Negative bias value	–50 Volts
Plate Dissipation	5.0 Watts
Peak Heater-Cathode Voltage	N/C
Maximum Grid Circuit Resistance	2.0 Megohms
Operating Temperature Range	–25°C to +125°C
Plate Current	30 mA

SIMILAR TS12AT7 FAMILY REPLACEMENT TYPES

12AU7, 6BC8, 6BQ7-A, 6CG7, 6J6, 7AU7, 9AU7, 8CG7, 12AV7, 6DT8, 6EV7, 12BZ7, 6201, 6679, 6189, 5814A, 6680, 6072, 396A, 407A, 407B, 12AX7, 12AZ7, 6BZ7, 6BZ8.

Foreign:

B152, B309, B739, ECC81, ECC82, E81CC, E82CC, ECC801, ECC801S, ECC802, ECC802S, ECC186, B329, B749, M8136, M8162, QB309, QA2406.

Physical Dimensions

.651/.639 DIA
.789/.771
.046 MAX
.260/.240
9 LEADS
.042/.038 DIA
.702/.698 DIA
.473/.463 DIA
36°

Connection Diagram

N/C 5
N/C 4
PT1 6
KT2 3
GT1 7
SOLID STATE ARRAY
GT2 2
KT1 8
PT2 1
N/C 9

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March 1973

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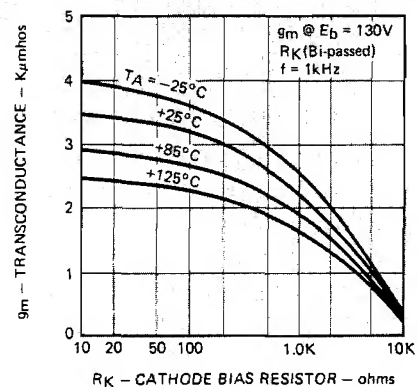
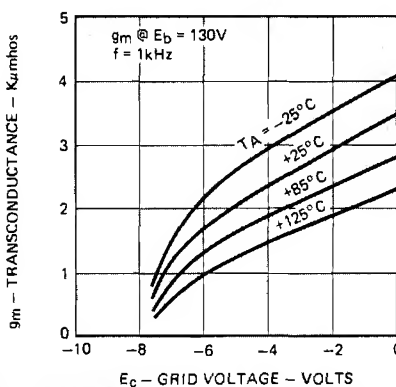
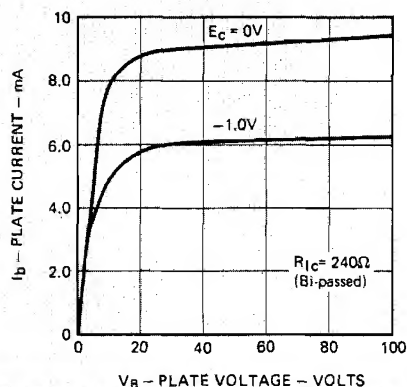
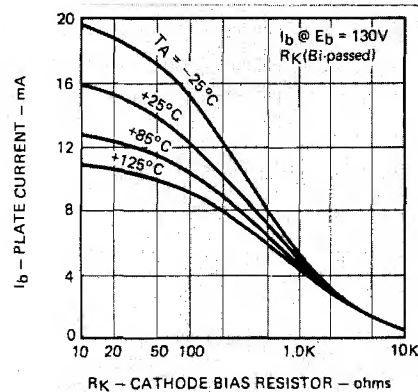
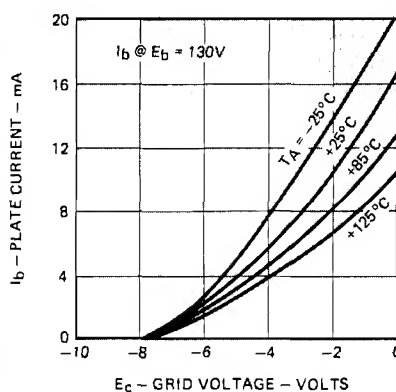
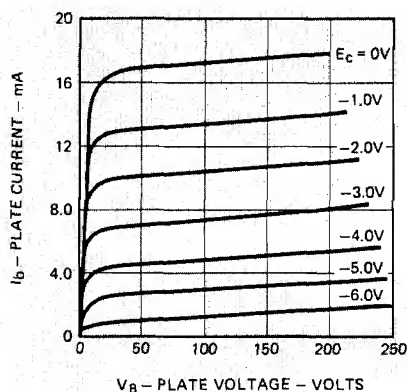
General Characteristics (Stated in conventional tube terminology)

Heater Voltage	N/C (Open)
Heater Current	N/C
Grid-to-Plate Capacitance (Each unit)	3.5μμF
Grid-to-Cathode Capacitance (Each unit)	25μμF
Plate-to-Plate Capacitance	0.1μμF
Heater-to-Cathode Capacitance	N/C

Operating Conditions and Characteristics (At 25°C unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Plate Supply Voltage	E_b		130	250	Volts
Cathode-Bias Resistor	R_K		240		ohms
Peak A-F Grid-to-Grid Voltage	E_{C1C2}			20	Volts
Plate Resistance	r_p	50	250		Kilohms
Transconductance	g_m	2000	3000	6000	Micromhos
Amplification Factor	μ	100	750		
Grid Voltage for Plate Current of 10μA			–7.0	–10	Volts
Peak Negative Grid Voltage	E_C	–150	–300		Volts
Plate Current	I_b	4.0	9.0	15	Milliamps
Grid Current	I_C		2.0	100	Nanoamps
Tube Operating Temperature	O_T	–55	+75	+125	°Centigrade

NOTE: In most cases, the more pentode type characteristics will enhance present circuit performance. In a few instances, the user might need a selected range.

Average Plate Characteristics (Each Unit)

NOTE: In series filament circuits, all tubes must be replaced by solid state replacements or appropriate resistor connected externally between pins 3 and 4. Some applications may require modified TS12AT7. Consult Teledyne Semiconductor for application information.

TELEDYNE SEMICONDUCTOR

TS12AX7*

*NOTE: Patent Pending.

TS12AX7*

Solid State Vacuum Tube Replacement

Features

- ZERO WARM-UP
- NO MICROPHONICS
- REDUCED HEAT RADIATION
- MECHANICALLY RUGGED
- TRUE CUTOFF WHEN USED AS SWITCH
- NO SCREEN GRID POWER
- SEMICONDUCTOR RELIABILITY
- LOW NOISE/DISTORTION
- DIRECT REPLACEMENT
- NO HEATER POWER
- NO TRANSCONDUCTANCE DEGRADATION WITH TIME

Description

The TS12AX7 is a 9-pin miniature twin triode in a metal hermetic sealed package. It is designed for direct replacement of the conventional glass vacuum tubes where greater reliability, stability, and performance are desired. It is used as multivibrators or oscillators in industrial control devices, phase inverters, clamp circuit, relay drivers, and other diversified applications. The low power consumption makes it ideal for mobile equipment tube replacement. Application is primarily intended for replacement in circuits requiring unusually low plate current operation, such as those employing the type 12AX7 vacuum tube. For other applications, refer to the **TS12AT7/A1** Fetron data sheet.

Maximum Ratings

Plate Voltage	250 Volts
Grid Voltage, Negative bias value	–50 Volts
Plate Dissipation	3.0 Watts
Peak Heater-Cathode Voltage	N/C
Maximum Grid Circuit Resistance	2.0 Megohms
Operating Temperature Range	–25°C to +125°C
Plate Current	5

SIMILAR TS12AT7 FAMILY REPLACEMENT TYPES

12AU7, 6BC8, 6BQ7-A, 6CG7, 6J6, 7AU7, 9AU7, 8CG7, 12AV7, 6DT8, 6EV7, 12BZ7, 6201, 6679, 6189, 5814A, 6680, 6072, 396A, 407A, 407B, 12AT7, 12AZ7, 6BZ7, 6BZ8.

Foreign:

B152, B309, B739, ECC81, ECC82, E81CC, E82CC, ECC801, ECC801S, ECC802, ECC802S, ECC186, B329, B749, M8136, M8162, QB309, QA2406.

Physical Dimensions

.651/.639 DIA
.789/.771
.046 MAX
.260/.240
9 LEADS
.042/.038 DIA
.702/.698 DIA
.473/.463 DIA
36°

Connection Diagram

N/C 5
PT1 6
GT1 7
KT1 8
N/C 9
PT2 1
GT2 2
KT2 3
N/C 4
SOLID STATE ARRAY

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April 1973

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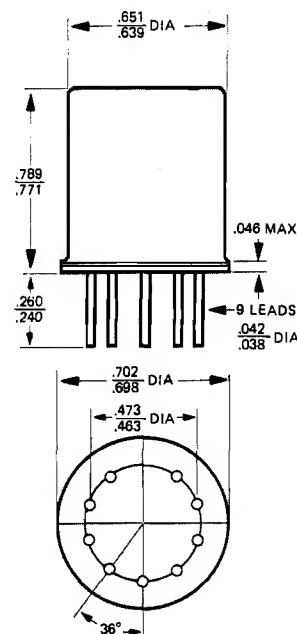
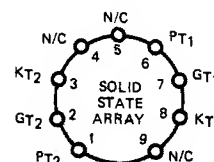
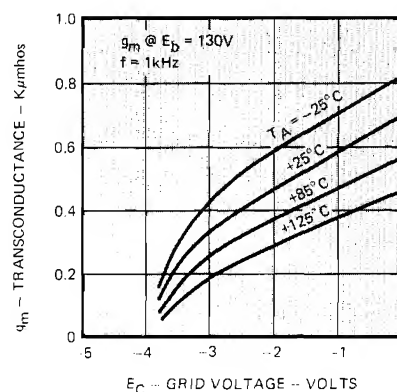
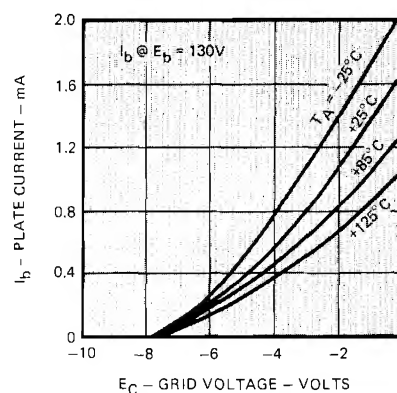
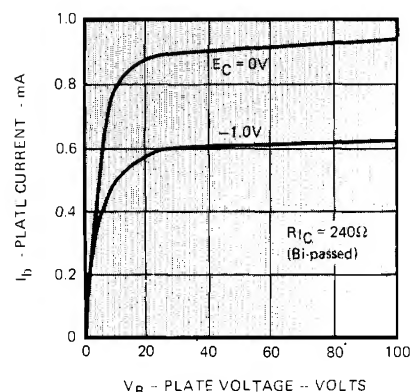
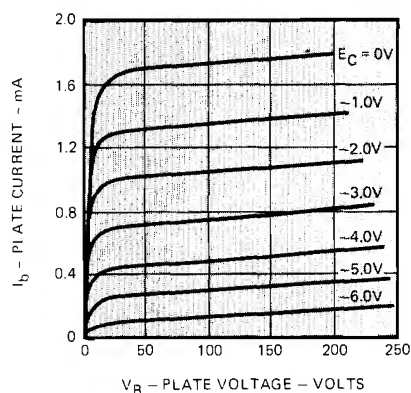

General Characteristics (Stated in conventional tube terminology)

Heater Voltage	N/C (Open)
Heater Current	N/C
Grid-to-Plate Capacitance (Each unit)	3.5$\mu\mu$F
Grid-to-Cathode Capacitance (Each unit)	2$\mu\mu$F
Plate-to-Plate Capacitance	0.1$\mu\mu$F
Heater-to-Cathode Capacitance	N/C

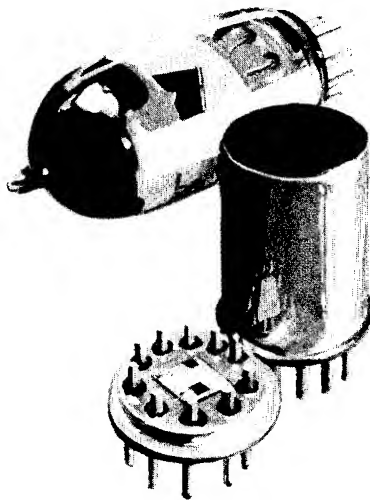
Operating Conditions and Characteristics (At 25°C unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Plate Supply Voltage	E_b		130	250	Volts
Grid No. 1 Voltage	E_{C1}	–0.3	–2.5	–2.7	Volts
Peak A-F Grid-to-Grid Voltage	E_{C1C2}			20	Volts
Plate Resistance	r_p	50	250		Kilohms
Transconductance	g_m	300	750	1000	Micromhos
Amplification Factor	μ	150	188		
Grid Voltage for Plate Current of 10μA			–7.0	–10	Volts
Peak Negative Grid Voltage	E_C	–150	–300		Volts
Plate Current	I_b	0.2	0.8	0.9	Milliamps
Grid Current	I_C		2.0	100	Nanoamps
Useful Frequency Limit	f_T		30		Megahertz
Tube Operating Temperature	O_T	–55	+75	+125	°Centigrade

NOTE: In most cases, the more pentode type characteristics will enhance present circuit performance. In a few instances, the user might need a selected range.

Average Plate Characteristics (Each Unit)

NOTE: In series filament circuits, all tubes must be replaced by solid state replacements or appropriate resistor connected externally between pins 3 and 4. Some applications may require modified TS12AT7. Consult Teledyne Semiconductor for application information.

FETRON application note 1

Vacuum tubes yield sockets to hybrid JFET devices

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TELEDYNE SEMICONDUCTOR

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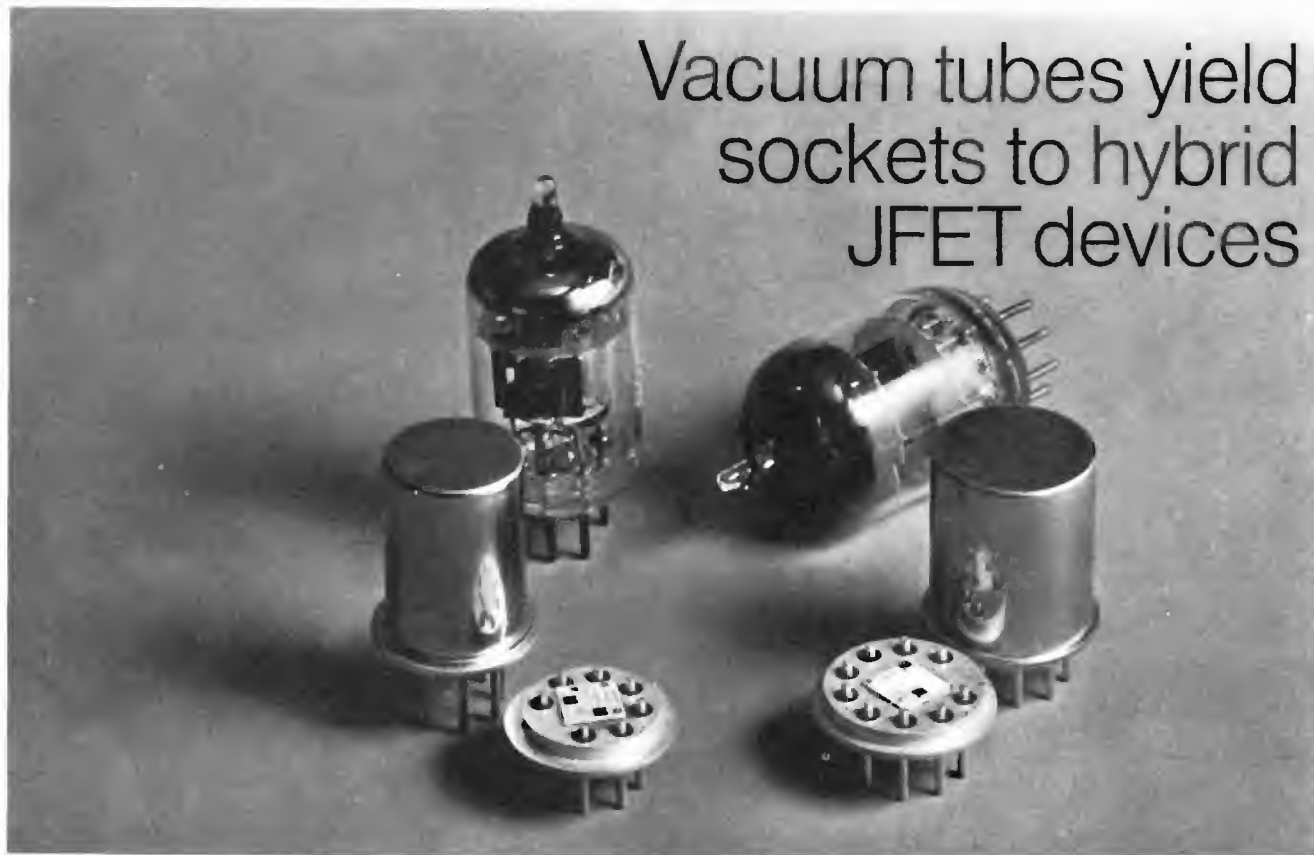
Vacuum tubes yield sockets to hybrid JFET devices

Thanks to high-voltage JFET technology, hybrid circuits called Fetrons exhibit virtually no aging, and also offer higher gain than do their vacuum tube counterparts

by Bruce Burman, *Teledyne Semiconductor, Mountain View, Calif.*

☐ A junction-field-effect device called a Fetron has been developed that replaces a vacuum tube in a circuit directly, without requiring major modifications in the circuit. To withstand the tube's high voltage supply (the B+ voltage), the device is built with the high-voltage JFET technology that was developed more than five years ago for military systems requiring breakdown voltages of 200 to 300 volts.

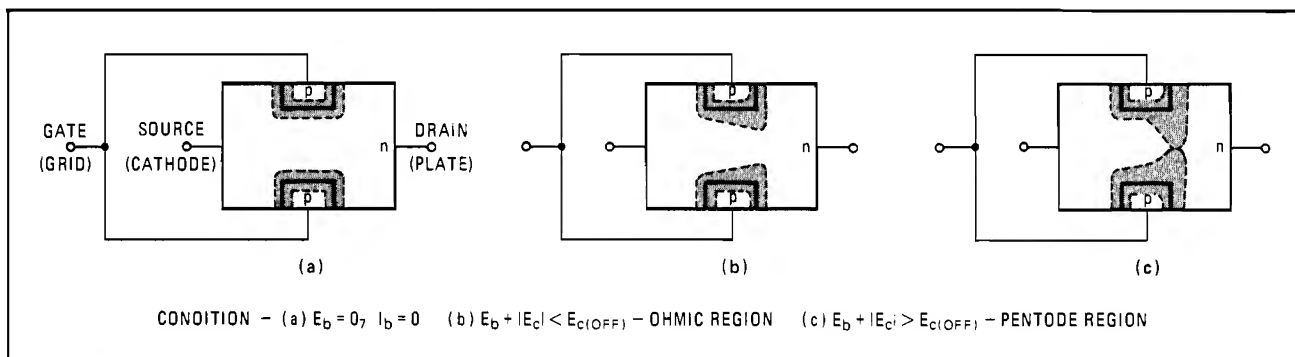
The Fetron package can be either a single JFET or two cascode-connected JFETs in a hybrid IC. Each kind is now being built as one-for-one replacements for such widely used tubes as the 6AK5 and 12AT7, and each goes into an oversized IC metal can that has the same pin configuration as the tube it replaces.

Why the Fetron?

From a design point of view, Fetrons make good sense as replacements for tubes in much communication equipment:

- Having no drift or aging, they can be locked in place for years, whereas the transconductance of many tubes degrades, often making monthly or quarterly adjustments and periodic replacements mandatory.
- Their improved performance includes higher amplification factors and lower noise than many tubes.
- Their low-power operation derives from the absence of heater or screen grids and the power supplies that run them. They also operate at 65 degrees centigrade, instead of the 100°C of tubes.
- The lifetimes of Fetrons are orders of magnitude longer than those of typical tubes—an estimated 30 million hours for Fetrons, 10,000 hours for tubes.
- They're physically tough, too—there's no glass to break in a metal can.

Fetrons make good sense in terms of sales, too. Billions of tubes that the Fetron could replace are still being used in communication and radar equipment. For instance, the utility telephone network in the U.S. alone contains about 150 million tubes within the Fetron's capabilities, creating approximately a $100 million-a-year market. And the maintenance bill of another major

Tubeless. Hybrid. JFET devices shown above replace tubes on one-for-one basis. Called Fetrons, they plug into unchanged circuit.

1. Brothers. JFET's elements are analogous to tube elements. The JFET source is comparable to the cathode, its drain to the plate, and gates to the grid. As the grid (plate) voltage goes negative, plate (drain) current drops. The gate's p-regions, growing into the channel, causes pinchoff, which is analogous to tube's cutoff.

telephone system's 50 million 6AK5 and 12AT7 tubes alone is estimated to be $500 million a year. Less than half that amount would be required to replace all these tubes with Fetrons once and for all. Then there are probably another 70 million pentode and triode tubes in use in other equipment that is regularly maintained and regularly tuned—from mobile radios to various types of industrial equipment. The potential market grows toward a billion dollars, without even considering consumer equipment.

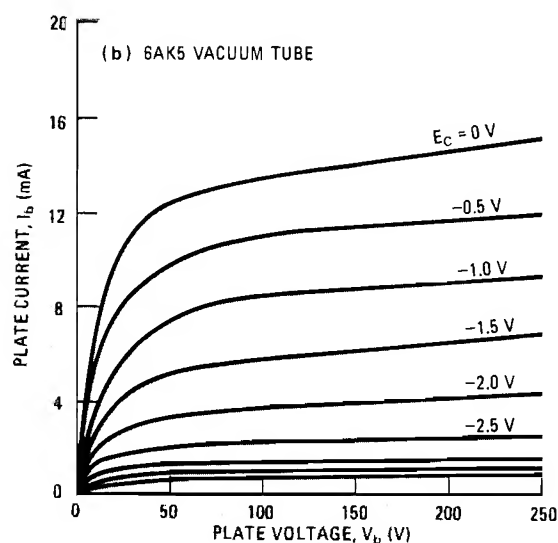
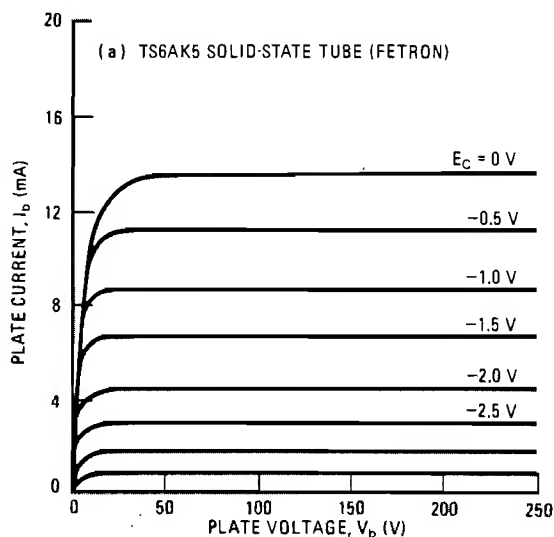
Viva la similarity

What makes the Fetron so attractive is that the JFET characteristics can be simply chosen to simulate a tube's dynamic performance. The circuit's normal trimmer components are used for high frequency tuning.

Basically, and very conveniently, a vacuum tube pentode and a JFET are brothers under the skin. Both are voltage-controlled devices and, if the differences between tube and transistor terminologies are ignored, both can be designed by using the same equations. Indeed, the operating polarities of n-channel JFETs and pentodes are identical, and they have similar output characteristics. If the JFET's drain and gate voltage are varied, the resultant family of curves will look just like the old familiar pentode plate-voltage-versus-plate-current curves at different values of control-grid voltage.

Even the current-control mechanisms of the two devices are analogous. In a tube, the grid voltage controls the number of electrons emitted from the cathode that reach the plate. In the JFET, the gate potential modulates conduction in a channel that exists between source and drain, as is shown in Fig. 1. The top and bottom gates of the JFET are comparable to the grid of the tube, its source is comparable to the tube's cathode, and its drain is comparable to the tube's plate. As the gate (grid) voltage goes negative, drain (plate) current drops because the gate (grid) p-regions grow into the n-channel region until they eventually pinch off the channel. This pinchoff is analogous to tube cutoff.

Again, the output characteristics of JFET and pentode are very similar, as can be seen in Fig. 2. But since the JFET has no elements comparable to the pentode's screen grid and suppressor grid, it is closer to the simpler triode in construction.

Since a JFET doesn't need a heater, warmup is instantaneous. Also, because of its lower inter-electrode capacitance and low channel resistivity, it can operate at

2. Equal but better. The JFET's output characteristics, although similar to those of a pentode, follow the square law more closely, and give a much cleaner on-off action, as is evident from the sharp cutoff.

much higher maximum signal frequencies than the tube, or at low frequencies with less distortion. The sharp cutoff evident in Fig. 2 gives a much cleaner on-off action, particularly in switching applications.

In short, the Fetron can be considered a better pentode than the vacuum tube pentode, because its drain output curves come much closer to the theoretical ideal.

And two JFETs are better than one

It requires two JFETs in a hybrid package to simulate the performance of one pentode. The JFET must withstand high plate voltage (see Fig. 2) to replace the tube directly. But there is no single high-voltage JFET with enough transconductance g_m to match that of the pentode tube. For example, to simulate the 6AK5 a transconductance of 3,500 to 7,500 micromhos at an operating current of 4 to 10 milliamperes is required.

Moderate g_m at high voltage is expensive to get with JFETs, since they must be physically large and of high-resistance material to yield high breakdown voltages. Then, too, the major barrier to high-frequency performance in semiconductors is the Miller effect—the gate-to-source capacitance. In an amplifier, Miller $C_{gs} = C_{gd}(1 + A)$. This is minimized in pentodes because of the extremely low plate-grid capacitance that exists because the control grid is shielded by the highly positive voltage screen grid.

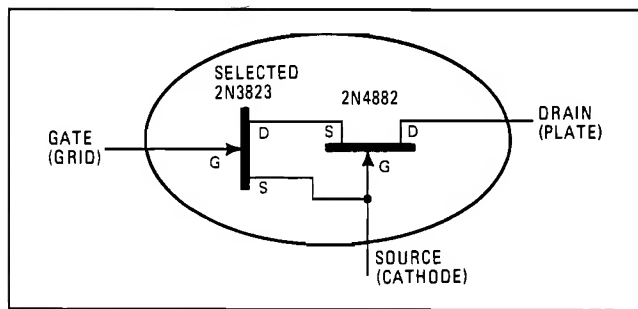
To get a high-transconductance, high-frequency (low-Miller-effect capacitance) JFET device, it's necessary to bootstrap or cascode two of them (Fig. 3). In such a design, the input transistor is a small-signal JFET, like the 2N3823, chosen for its low capacitance and high g_m; the output device is a high-voltage JFET, such as a 2N4882. The pair is assembled as chips and packaged in cans.

Smooth operator

The operation of the hybrid assembly is simple. The output JFET reduces the plate voltage to a safe level for the input JFET. The former JFET's drain is always connected to the high voltage—the equivalent plate connection in a Fetron—and its gate source connected to the input JFET's gate, which is tied to a low voltage or ground. With this arrangement the input capacitance of the device is just the fairly low capacitance of the input JFET, rather than the much higher capacitance associated with the large high-voltage chip.

With this arrangement assuring equal gains, the Miller-effect capacitance is equal to or lower than that of a tube pentode. The Fetron has only the 0.02-picofarad drain-to-source capacitance of the high-voltage JFET in series with the drain-to-gate capacitance of the unity-voltage-gain low-voltage input JFET. The result: less than 0.02-pF Miller-effect capacitance.

Also, the cascode arrangement boosts the effective output impedance of the Fetron about an order of magnitude above that of a pentode tube. This not only greatly improves the pentode curves, but makes the circuit gain less dependent on Fetron characteristics.

The device's input looks like a reverse-biased semiconductor junction, which provides a very high resistance that's desirable in most applications. Significantly, the effective input impedance is an order of magnitude above a vacuum tube's. This enables a circuit to operate from a high-resistance source without being loaded down.

3. Gaining with cascodes. Most Fetrons are built with two JFETs in a bootstrap or cascode connection to achieve high-gain operation. Miller-effect capacitance is minimized by using a low-capacitance, high-gain input transistor, such as the 2N3823, connected to a high-voltage 2N4882 output device.

Amplification equations

The tube equations apply when the Fetron is plugged into a typical tube biasing network, like the one shown in Fig. 4. (Heater and extra grid connections are left open on the Fetron.)

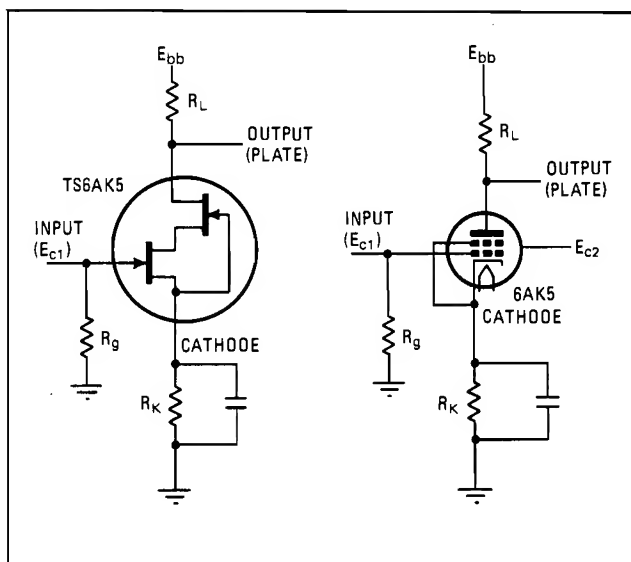
At any control grid voltage, the plate current will be

$$I_b = I_{b0}\left[1 - \frac{E_c}{E_{c(off)}}\right]^2$$

where

I_{b0} = plate current at $E_c = 0$ V
I_b = plate current at E_c voltage
E_c = control grid voltage
$E_{c(off)}$ = E_c for 1 μA of I_b

The change of plate current with grid voltage at a constant plate current gives the transconductance. By differentiating the equation for plate current with respect to control voltage:

$$g_m = \frac{\Delta I_b}{\Delta E_c}\Bigg|_{E_b = K} = g_{m0}\left[1 - \frac{E_c}{E_{c(off)}}\right]$$

4. Same old circuit. A Fetron (TS6AK5, for example) can directly replace a tube (6AK5, for example) in an unaltered circuit. The heater and extra grid connections are left open on the Fetron.

where g_m = transconductance at operating E_c, and g_{m0} = transconductance at $E_c = 0$ V.

These characteristics give the solid-state device a true square-law characteristic and, because of this, very low harmonic distortion. Higher-than-second-order harmonics are virtually nonexistent.

In contrast, the vacuum tubes have a "three-halves-power" characteristic, and can generate substantially higher-order harmonics and intermodulation products. Interestingly enough, bipolar transistors have even more harmonics than the tube.

The Fetron's very high output impedance, analogous to a vacuum tube's plate resistance r_p, maximizes the voltage gain for a given load R_L. The voltage gain of an amplifier (see Fig. 4) can be expressed as:

$$A_v = \frac{\mu R_L}{r_p + R_L} = \frac{g_m r_p R_L}{r_p + R_L}$$

where $\mu = g_m r_p$ (μ is the tube amplification factor). But since r_p is much higher than R_L, the equation is simply

$$A_v \approx g_m R_L$$

At lower frequencies—less than a few megahertz—the simplified equation is more than 99% accurate for a Fetron.

Fitting the FETs

Versions of the device can be made for both amplifier and oscillator service. (The package for oscillator applications may include a small resistor or RC network for feedback and neutralization.) In practice, many FET characteristics are available, and single or JFET cascode pairs can be made to match the tube's current-voltage curves as shown in Fig. 5.

Although several approaches are available, about 80% of the general-purpose applications considered to date are satisfied by the simple FET #1 approach. This type of JFET is chosen if the application is unknown or if the device must operate around some nominal operating point A (in which case, the JFET curve closely approximates the tube curve over most of the control voltage range). In large-volume applications, where the exact operating point is known, FET #1 can be selected at the factory to coincide exactly with a point anywhere near A on the tube's curve.

An operating point such as B beyond the normal FET cutoff can be matched by FET #2 or FET #3. FET #2 would provide a higher current for the same control voltage, so it passes through B before cutoff. FET #3 would have to be specially tailored for low, flat current characteristics, or for a narrow range of operation beyond the normal FET's cutoff. It would be a lower-transconductance, higher-cutoff JFET.

In simulating a tube, the dynamic characteristics as well as the operating point must be considered. Depending on the particular application, special attention must be given to transconductance, phase shift, phase margin, operating range, and neutralization requirements.

For amplifier operation, neutralization and operating range are the principle concerns. In most tube circuits, neutralization is used to nullify the effects of feedback capacitance during higher-frequency operation.

When used as an oscillator, the Fetron must provide for positive feedback between the output and input. An internal RC network within the device headers (Fig. 6) acts as a screen grid which is connected to the plate to assure direct replacement.

In Fetrons designed for amplifier operations, how-

5. Choosing a Fetron. Several Fetron types are available to match a tube's application. If the tube operates around a fixed point, such as A, a JFET, such as FET #1, is chosen. To match a tube that operates beyond a FET's cutoff, FET #2 or FET #3 is chosen: FET #2 for high current before cutoff, FET #3 for low, flat current.

Building the high-voltage JFETs

JFETs with breakdown voltages over 300 volts can be made by standard planar processing. But to achieve this high voltage, it is essential to attain the maximum breakdown field for silicon, about 30 volts per micron. Also critical is the epitaxial layer thickness and resistivity.

The channel is formed by the n-type epitaxial layer, which has a resistivity exceeding 5 ohm-cm. Since the channel region where pinchoff occurs is directly under the gate, doping levels in that region must be precisely controlled to limit spreading of the depletion region into the channel. The channel height depends on what final pinchoff voltage is desired.

The voltage from gate to source, V_{GS}, may be as large as –50 V. This V_{DG} value is required to enable the drain to withstand a voltage of up to 400 V. However, this high drain-to-gate voltage can only be achieved if the spacing of the gate, source and drain is held to very close tolerances.

Another difficulty is the need to shape the diffusions so as to minimize any surface field concentrations at the chip. Breakdown should occur in the bulk silicon, not at the surface. The substrate resistivity must be fairly high for good control of depletion spreading, as well. Otherwise, the channel might get pinched off with a very small charge in V_{GS}. At high operating voltages, V_{DS} can vary widely without any change in signal voltage, due to normal supply tolerances.

ever, the RC network is omitted. If needed, a capacitor is added to provide the necessary frequency response. Characteristics of a properly trimmed TS6AK5 Fetron and the tube it replaces are listed in Table 1. Heater voltage is not specified, because those pins are not connected in the Fetron.

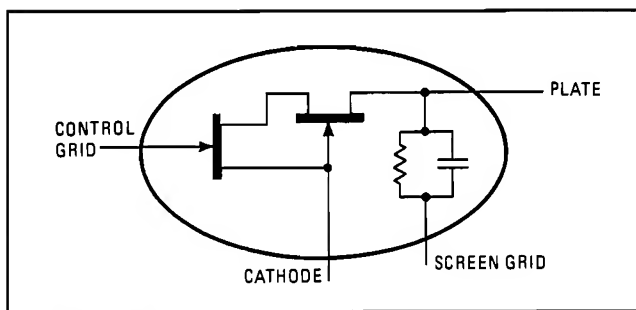
Note the great increases in amplification factor and plate resistance when Fetrons are used. The effect of these differences on the circuit is greatly improved sensitivity—about 4 to 5 decibels—resulting from the higher $m\mu$, lower noise, and low distortion.

Triode simulation

The Fetron will also perform well if configured as a triode, for the three electrodes of a single JFET directly simulate the latter's grid, cathode, and anode. But the JFET's much higher output impedance (hence higher gain) could cause an amplifier circuit to oscillate. Usually, however, the load resistance of a circuit is much smaller than r_p of the Fetron, and there is no problem.

The first Fetron triodes made were equivalents of the 12AT7 and Western Electric's 407 version, which has a 20-volt heater and slightly different pin-out. These Fetrons operate as twin triodes. Figure 7 and Table 2 show their characteristics compared to a single triode. Although the Fetron's transconductance is significantly lower (each of the triodes is a single high-voltage FET), its transconductance is the same as that of the twin triode being replaced. And the design equations given for pentode amplifiers also apply to the triode version.

True, the Fetron output characteristics approximates a pentode's, not a triode's. But it can be used to replace a twin triode—the more common triode application because two of the small inexpensive devices go easily into one glass tube envelope. It's generally not as good an electronic device as a pentode, though many circuit designers use them in cascode to get lower noise than obtainable with a pentode. Now, the Fetron triode upgrades typical circuit performance because of its excellent square-law characteristics throughout the control voltage range. Power supply regulation can also be relaxed—triodes normally require well-regulated power supplies, because triode operating current depends on operating plate voltage, whereas the Fetron's does not (see Fig. 7a).

CONTROL GRID
PLATE
CATHODE
SCREEN GRID

6. Farflung net. This oscillator network is used when Fetrons replace a pentode oscillator. The resistor and/or resistor-capacitor combination simulates screen-grid action. The network is included within the header, permitting 1:1 replacement.

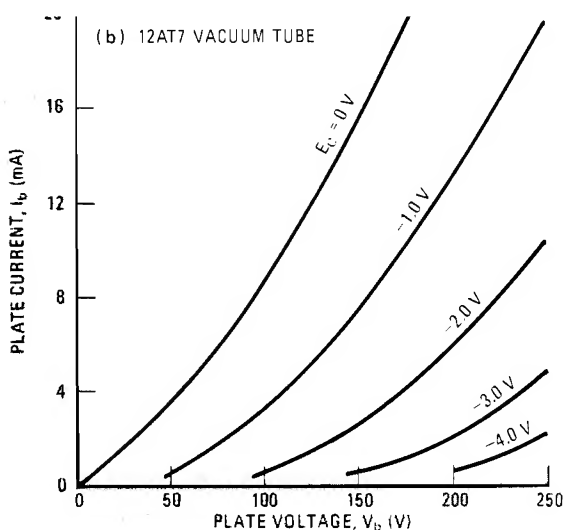
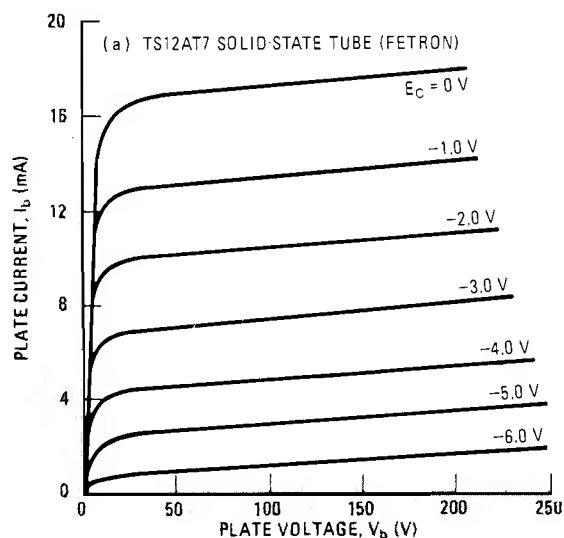
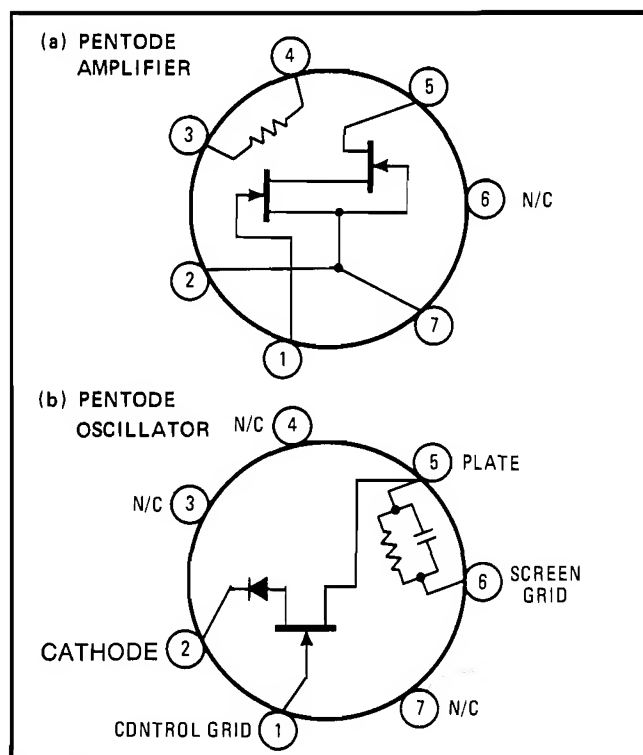
It's dependable

Besides replacing pentode and triode tubes, the Fetron gets higher marks in reliability than either. A high-reliability tube has a life expectance of 5 × 10^4 hours (63% failure point). Preliminary data from burn-in and accelerated life tests on 1,000 Fetrons indicates a life expectancy of 3 × 10^6 hours, or 300 years. Of the 1,000 in the sample, 787 were screened by the type of power burn-in tests generally given high-reliability tubes, and were operated for 20 hours at twice normal dissipation (1,760 milliwatts). The failure rate, or dropout, was only 3.5%, a small fraction of the tube screening dropout rate.

In addition, some 2,500 Fetrons have been shipped to telephone companies for evaluation and trial applications. Many have been in use for as long as eight months, and to date, failures or degradations reported have been statistically unimportant.

Finally, another group was put in a 170° C oven and

(a) TS12AT7 SOLID-STATE TUBE (FETRON)
E_C = 0 V
−1.0 V
−2.0 V
−3.0 V
−4.0 V
−5.0 V
−6.0 V
PLATE CURRENT, I_b (mA)
PLATE VOLTAGE, V_b (V)

(b) 12AT7 VACUUM TUBE
E_C = 0 V
−1.0 V
−2.0 V
−3.0 V
−4.0 V
PLATE CURRENT, I_b (mA)
PLATE VOLTAGE, V_b (V)

7. Just like a triode. Although the characteristics of a Fetron are different from those of a typical triode, they are similar to those of a triode pair and can be used wherever twin triodes are used. In fact, Fetrons were first designed to replace Western Electric's 407 twin triode.

8. Different configurations. The internal configurations depend on whether the Fetron is destined for service as a pentode amplifier (a) or oscillator (b). For oscillator use, an internal RC network provides the required feedback when the Fetron is plugged into sockets.

powered at 1.2 W, a test that keeps the junction temperature at 215°C for 450 hours. One failed and one degraded (leaked), indicating device survival at 25°C for 10^{11} hours.

From these destruction tests, it was found that although normal operating current is 7 mA, it generally takes a steady current above 30 mA, at 350 to 400 V, to induce failure. Surges up to 6 A can be withstood. Internal connections melt at 9 to 10 A, but fusing links can be built into the device so that if it does fail catastrophically, the circuit is protected.

Shock and other physical tests, comparable to normal IC environmental tests, have also been made. The Fetron, because of its hard metal case, is virtually unbreakable. The case is a solid, deep-drawn steel cap welded to a large header. Before welding, the case is evacuated and backfilled with dry nitrogen.

Almost every general-purpose pentode and triode tube type, and various special-purpose ones, may be simulated with Fetrons, by selecting the appropriate FET pair and varying the internal connections and networks. Figure 8 shows two versions.

Variations include:

- The standard amplifier (6AK5 with 6.3-V heater). In amplifier circuits, a cathode resistor is commonly used to adjust the operating point. At frequencies up to 30 MHz, amplifiers don't need a neutralization network. At higher frequencies, an adjustable capacitor is usually available in the circuit. If not, a 2-pF capacitor may be added internally or externally.
- The oscillator, with the screen grid simulated and feedback to input provided by the connection to pin 6.
- The low-gain single-FET pentode.
- The twin-triode amplifier, for low-noise cascoded triode circuits.
- The twin triode, with an RC network inserted for voltage regulator circuits.

The Fetron pentodes have been operated to 500 MHz, exhibit lower i-f noise than the original tubes, and do not suffer from microphonics. Elimination of heater power, and usually all screen grid power as well, cuts supply drain and reduces operating temperature from well over 100°C for the tubes to about 650°C for the Fetron. After some eight months of trial operation, there has been no noticeable degradation in its transconductance.

Fetron triodes will generally be used in low-frequency applications. In most of these, their sharp cutoff improves on the original circuit performance. Naturally, such triodes have the same general noise and power-saving advantages as the Fetron pentodes.

Pacific Telephone Co. recently has converted to Fetrons on a trial basis in a number of repeater lines between San Francisco and Martinez, Calif. In addition, some of the channel equipment for multiplexing and

TABLE 1: TYPICAL PENTODE DEVICE CHARACTERISTICS – R_K = 200 Ω, E_b = 120 V

PARAMETER	UNITS	6AK5 VACUUM	TS6AK5 SOLID-STATE
Plate voltage breakdown	V	350	350
Plate resistance	MΩ	0.5	5.0
Transconductance	μmhos	5,000	4,500
Plate current (R_K = 200 Ω)	mA	7.5	7.0
Grid voltage for I_b = 10 μA	V	−8.5	−5.0
Amplification factor	–	2,500	22,500
Input capacitance	pF	4.0	6.5
Output capacitance	pF	0.02	0.02
Useful frequency limit	MHz	400	600

TABLE 2: TYPICAL TRIODE DEVICE CHARACTERISTICS (EACH SIDE) — R_K = 240 Ω, E_b = 130 V

PARAMETER	UNITS	12AT7 VACUUM	TS12AT7 SOLID-STATE
Plate voltage breakdown	V	400+	350
Plate resistance	kΩ	15	250
Transconductance	μmhos	4,000	3,000
Plate current (R_K = 240 Ω)	mA	5.0	9.0
Grid voltage for I_b = 10 μA	V	−7.0	−7.0
Amplification factor	—	60	750
Input capacitance	pF	2.2	25
Output capacitance	pF	1.5	3.5

demultiplexing in a carrier office is now equipped with Fetrons.

What next?

There are numerous tube types that can be made with the basic Fetron designs. Types such as the 6JC6 and 6EW6, which have transconductances in the vicinity of 25,000 micromhos and plate currents in the 40-mA range and which have already been made, can be combined with the 6AK5, 12AT7, and their derivatives so as to make Fetron versions of the great majority of popular tube types. Next to be tackled will be the power pentode devices, such as 6AQ5, 6V6, and remote cutoff pentodes, such as 6BA6. Indeed, with volume production and some packaging changes, the Fetron could go on to become a low-cost replacement for most tubes. □

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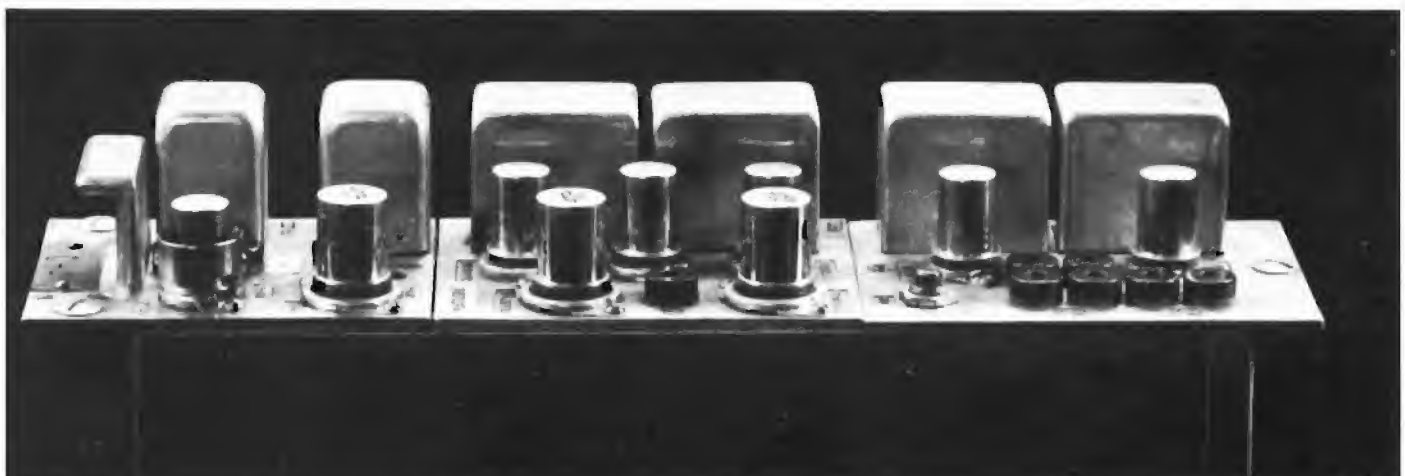
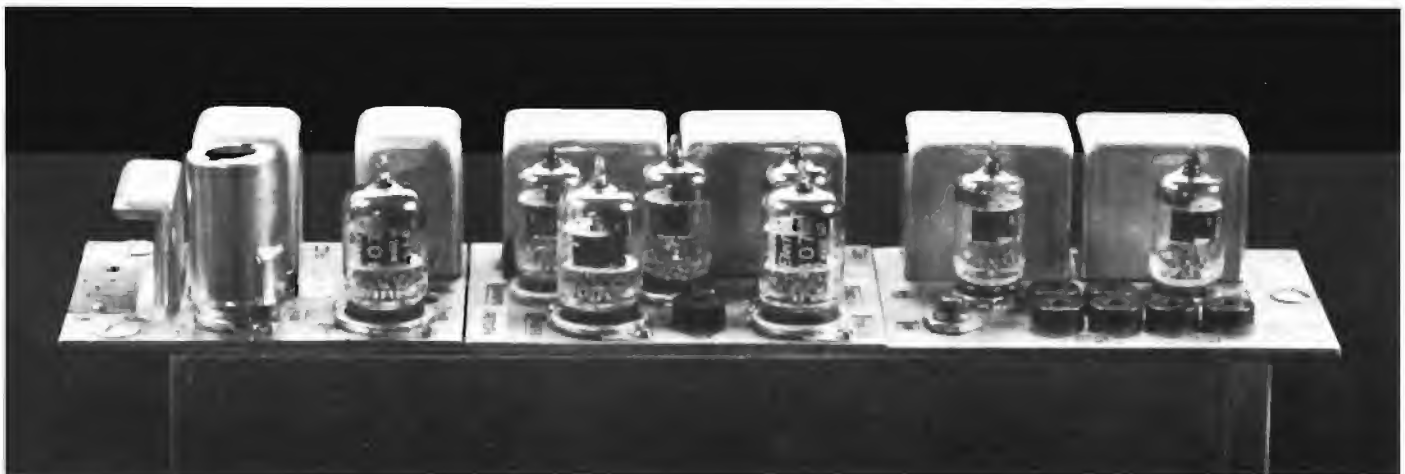
2. R. L. Berger, "The Direct Replacement of Pentode Vacuum Tubes with Cascode Field Effect Transistors," Mid-America Electronics Conference, Kansas City, Mo., October, 1971.

9. Finding their place. In the above amplifier, all the 6AK5 and 12AT7 tubes have been replaced with equivalent Fetrons.

february 1974

application note

FETRON application note no. 2: FETRON Test Fixture

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A Simple Fixture for Field Testing FETRONs

Assemble the test jig shown in Figure 1 which is wired according to the schematic shown in Figure 2.

After attaching a power supply and connector, the FETRON is inserted in the socket according to the socket callout in Tables I or II. With the cathode resistor switch in the "in" position, read the current referred to as Idsr in Tables I or II. To show that the device has gain, throw the cathode resistor switch to the "out" position. The current should roughly double in value. A good approximation of the transconductance may be computed at this point using the equation:

$$gm = \frac{\frac{I_C}{I_O} - 1}{R_K}$$

Where R_K = 200Ω for S1 and 240Ω for S2 and S3.

I_C = Drain current with cathode bypass switch (S1, S2 or S3) closed.

I_O = Drain current with cathode bypass switch open.

This equation is verified in Appendix I.

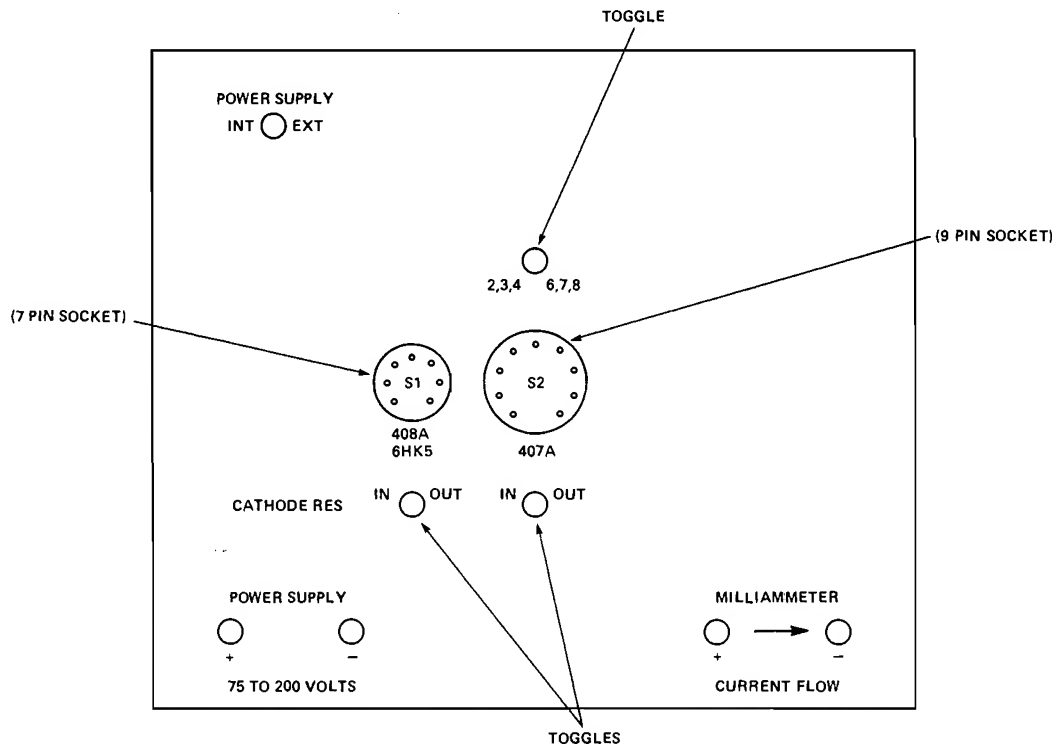



Figure 1. FETRON Test Fixture.

TABLE I.

FETRON	Tube	Idsr	gm	R_K	Side	Idsr	gm	R_K	Side	Comments	Socket
1005	407A	0.505 to 2.25	.35 Min.	240	2,3,4	3.0 to 11.0	1.8 to 6.0	240	6,7,8		S2
1008	407A	4.0 to 10.0	2.5 - 6.0	240	2,3,4	4.0 to 10.0	2.5 to 6.0	240	6,7,8		S2
1022	407A	2.0 to 6.0	2.5 Min.	240	2,3,4	2.0 to 6.0	2.5 Min.	240	6,7,8	Both sides cascoded	S2
1023	407A	.041 to 0.21	.4 Min.	240	2,3,4	.041 to 0.21	.4 Min.	240	2,3,4		S2
1024	407A	.4 to 2.0	.35 Min.	240	2,3,4	.4 to 2.0	.35 Min.	240	6,7,8		S2
1030	407A	3.0 to 10.0	2.2 - 6.0	240	2,3,4	2.0 to 5.5	1.5 Min.	240	6,7,8		S2
1032	407A	4.0 to 15.0	2.5 to 6.0	240	2,3,4	4.0 to 15.0	2.5 - 6.0	240	6,7,8		S2
1033	407A	3.6 to 7.3	3.5 Min.	240	2,3,4	3.5 - 11.0	2.0 Min.	240	6,7,8	2,3,4 = case	S2
1037	407A	0.45 to 1.37	.35 Min.	240	2,3,4	3.0 - 11.0	1.8 to 6.0	240	6,7,8		S2
1038	407A	3.0 to 11.0	1.8 to 6.0	240	2,3,4	.42 to 2.1	.35 Min.	240	6,7,8		S2
1042	407A	1.5 to 3.1	.35 Min.	"0"	2,3,4	3.0 to 11.0	1.8 to 6.0	240	6,7,8		S2
1044	407A	.41 to 2.0	0.3 to 1.0	240	2,3,4	.41 to 2.0	0.3 to 1.0	240	6,7,8		S2
1046	407A	4.0 to 15.0	2.5 to 6.0	240	2,3,4	4.0 to 15.0	2.5 to 6.0	240	6,7,8		S2
1077	407A	10 to 30	3.0 to 7.0	"0"	2,3,4	8 to 18.0	3.0 to 7.0	"0"	6,7,8	Regulator	S2

TABLE II.

FETRON	Tube	Idsr	gm	R_K	Comments	Socket
1000	408A	5.0 to 9.0	4.0 to 7.2	200	3 - 4 Sht.	S1
1001	408A	4 to 10	3.9 to 8.0	200		S1
1011	408A	4 to 10	3.5 to 7.5	200	Cathode diode	S1
1013	408A	4 to 10	3.5 to 7.5	200	6AK5	S1
1018	408A	7 to 12	3.9 to 8.0	200		S1
1029	408A	3 to 9	4.0 to 7.2	200		S1
1035	408A	5 to 9	4.0 to 7.2	200		S1
1036	408A	4 to 12	4.0 to 10.0	200		S1
1003	408A	2 to 5.5	2.5 to 7.0	200		S1
1012	408A	2 to 5.5	2.5 to 7.0	200		S1
1019	408A	2.0 Min.	3.5 Min.	200	Oscillator	S1
1049	408A	3.0 to 8.0	3.5 to 8.0	200	Also 2.5 to 6.0, 2.0 - 6.0, 200 Oscillator	S1
1004	408A	.04 to 0.2	.35 Min.	200		S1
1039	408A	.4 to 1.8	.35 Min.	200		S1
1040	408A	1.5 to 5.5	2.0 to 8.0	200		S1
1014	408A	4 to 10	1.9 to 5.9	200	Has second gate on pin 7	S1
1056	408A	4 to 10	1.9 to 5.9	200	Same as TR1014	S1

EXTERNAL POWER SUPPLY

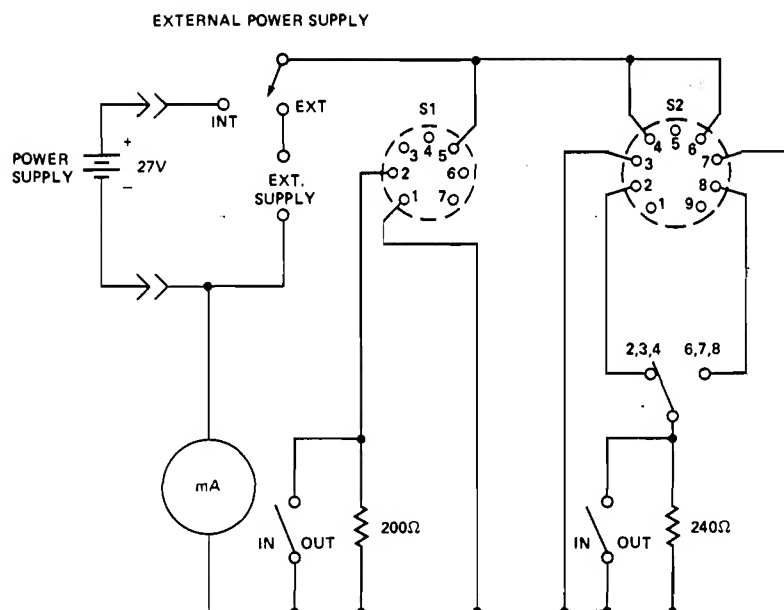



Figure 2. FETRON Test Fixture Schematic.

APPENDIX I. TRANSCONDUCTANCE MEASUREMENTS

Transconductance can be calculated from currents monitored with a simple DC FETRON testor by means of the equation:

$$gm = \frac{\frac{I_c}{I_o} - 1}{R_K}$$

Where referring to the schematic shown:

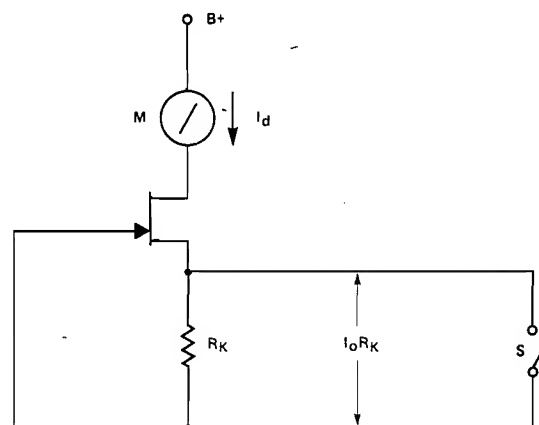
R_K is the cathode resistor.

I_o is the current with switch S open.

I_c is the current with switch S closed.

$$gm \triangleq \frac{\Delta I_d}{\Delta V_g} \qquad \therefore gm = \frac{I_c - I_o}{I_o R_K} = \frac{\frac{I_c}{I_o} - 1}{R_K}$$

$I_d = I_c - I_o$ for switch alternately open and closed.

$\Delta V_g = I_o R_K$ for switch alternately open and closed since $V_g = 0$ for SW closed.

This method gives only "Large Signal" gm and should be interpreted only as a first order approximation to small signal gm.

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Instrument Conversion Kits

HP400 Voltmeter
Tektronix Oscilloscope CA Plug-in Module

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A sure cure for vacuum-tube aging and associated reliability problems in instruments, and for the resulting calibration, maintenance and inventory expenses, is a FETRON® solid-state tube conversion kit from Teledyne Semiconductor.

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Communications companies are using FETRONs in large quantities to improve existing tube equipment. Now for the instrument owner, Teledyne has developed off-the-shelf conversion kits. Each is a set of FETRONs designed to replace the tubes in widely used instruments.

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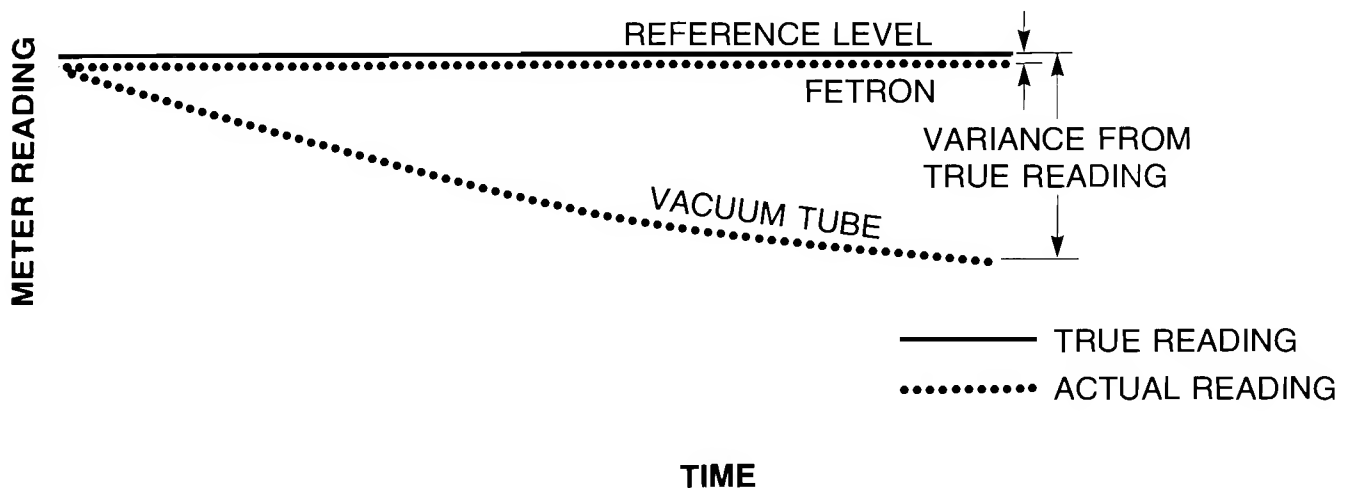
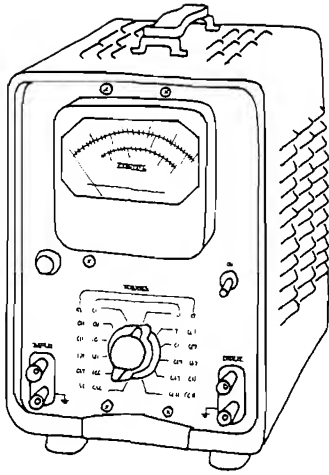
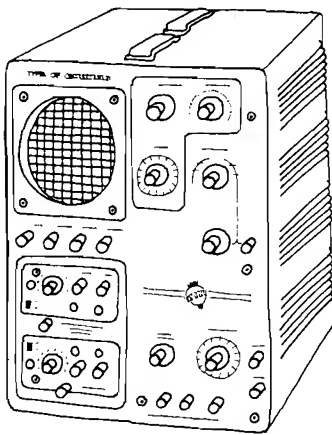
Solid-State Stability and Reliability

By retrofitting with FETRON conversion kits from Teledyne, you can extend the useful life of a vacuum-tube instrument many years and stretch out calibration intervals beyond 12 months.

Improved Accuracy. FETRONs never drift, but vacuum tubes begin drifting immediately causing greater errors between calibrations. With FETRONs, periodic calibration is required only as a check for malfunctions.

METER READING
REFERENCE LEVEL
FETRON
VARIANCE FROM TRUE READING
VACUUM TUBE
TRUE READING
ACTUAL READING
TIME

The graph shows the difference in stability between vacuum tubes and FETRONs, as measured on a VTVM before and after conversion. Since drift is eliminated, the normal three-month recalibration cycle can be replaced by a cycle of 12 months or longer, with occasional bench checks to make sure the instrument is functioning properly.

Being solid-state, FETRONs are not subject to tube degradation modes, such as gassiness, microphonics and filament deterioration, that upset measurement accuracy. What's more, FETRONs are immune to shock and vibration levels that could damage tubes, and they have many, many times the operating lifetime of tubes. They also improve the overall reliability of the instrument because they run cool, without heater power.

HP400 Conversion Kit

The HP400 conversion kit replaces the five amplifier circuit tubes of the HP400 VTVM. Conversion consists of removing the tubes, plugging in the FETRONs, and recalibrating the instrument with step-by-step procedures given in the instruction booklet.

CA Plug-in Conversion Kit

This kit replaces all 15 tubes in the CA plug-in module for Tektronix 500 series oscilloscopes. In addition to replacing the tubes, minor wiring changes are required. An instruction booklet details the conversion steps.

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